Chapter 1 Homework Solutions

1.1-1 Using Eq. (1) of Sec 1.1, give the base-10 value for the 5-bit binary number 11010 ($b_4\ b_3\ b_2\ b_1\ b_0$ ordering).

From Eq. (1) of Sec 1.1 we have

$$b_{N-1}\,2^{-1} + b_{N-2}\,2^{-2} + b_{N-3}\,2^{-3} + \cdots + b_0\,2^{-N} = \sum_{i=1}^{N} b_{N-i}2^{-i}$$

$$1\times 2^{-1} + 1\times 2^{-2} + 0\times 2^{-3} + 1\times 2^{-4} + 0\times 2^{-5} = \frac{1}{2} + \frac{1}{4} + \frac{0}{8} + \frac{1}{16} + \frac{0}{32}$$

$$= \frac{16 + 8 + 0 + 2 + 0}{32} = \frac{26}{32} = \frac{13}{16}$$

1.1-2 Process the sinusoid in Fig. P1.2 through an analog sample and hold. The sample points are given at each integer value of t/T.

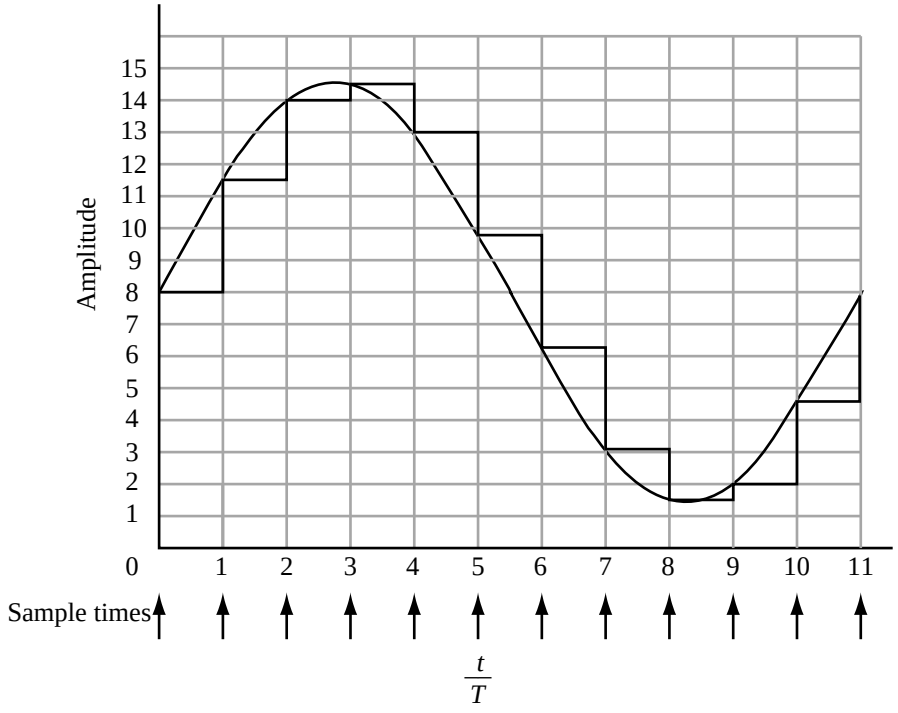


Figure P1.1-2

1.1-3 Digitize the sinusoid given in Fig. P1.2 according to Eq. (1) in Sec. 1.1 using a four-bit digitizer.

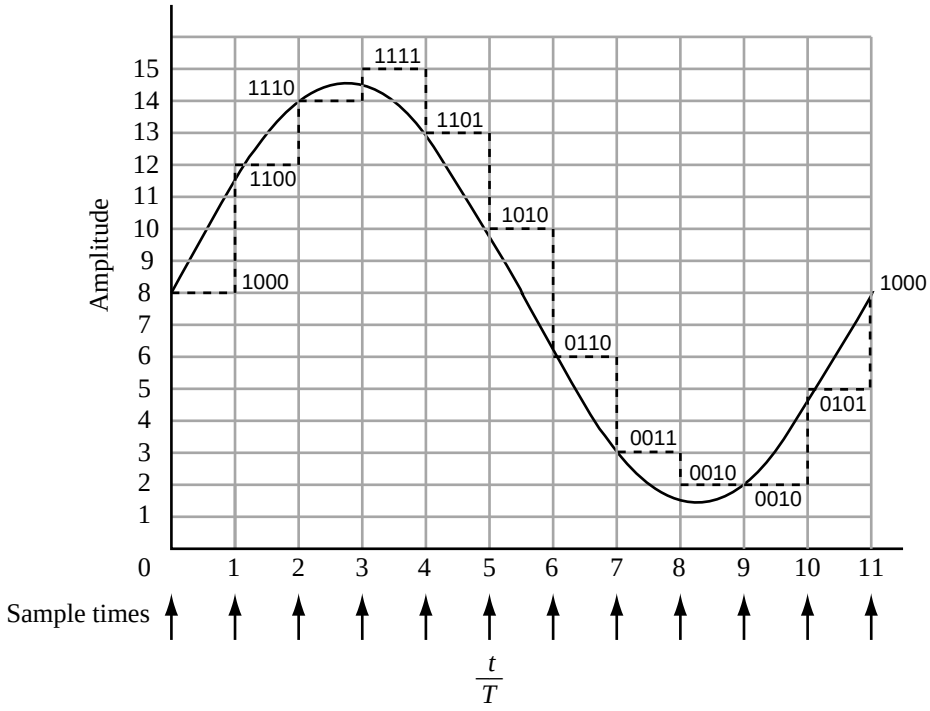


Figure P1.1-3

The figure illustrates the digitized result. At several places in the waveform, the digitized value must resolve a sampled value that lies equally between two digital values. The resulting digitized value could be either of the two values as illustrated in the list below.

Sample Time	4-bit Output
0	1000
1	1100
2	1110
3	1111 or 1110
4	1101
5	1010
6	0110
7	0011
8	0010 or 0001
9	0010
10	0101
11	1000

1.1-4 Use the nodal equation method to find v_{out}/v_{in} of Fig. P1.4.

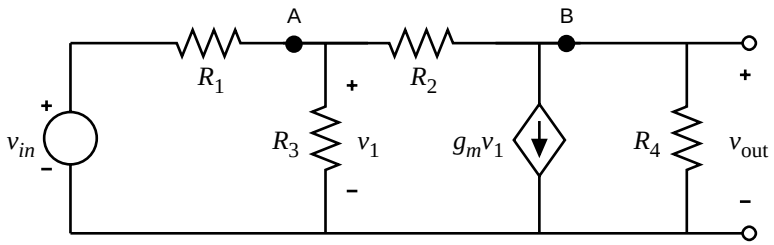


Figure P1.1-4

Node A:

$0 = G_1(v_1 - v_{in}) + G_3(v_1) + G_2(v_1 - v_{out})$

$v_1(G_1 + G_2 + G_3) - G_2(v_{out}) = G_1(v_{in})$

Node B:

$0 = G_2(v_{out} - v_1) + g_{m1}(v_1) + G_4(v_{out})$

$v_1(g_{m1} - G_2) + v_{out}(G_2 + G_4) = 0$

$$v_{out} = \frac{\begin{vmatrix} G_1+G_2+G_3 & G_1 v_{in} \\ g_{m1} - G_2 & 0 \end{vmatrix}}{\begin{vmatrix} G_1+G_2+G_3 & -G_2 \\ g_{m1} - G_2 & G_2 + G_4 \end{vmatrix}}$$

$$\frac{v_{out}}{v_{in}} = \frac{G_1 (G_2 - g_{m1})}{G_1 G_2 + G_1 G_4 + G_2 G_4 + G_3 G_2 + G_3 G_4 + G_2 g_{m1}}$$

1.1-5 Use the mesh equation method to find v_{out}/v_{in} of Fig. P1.4.

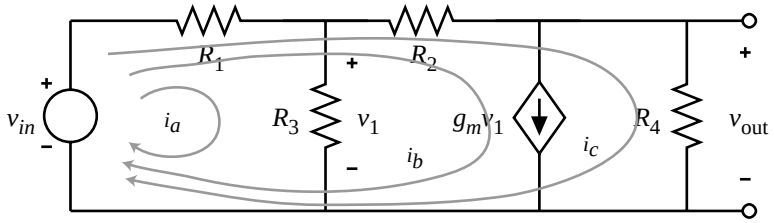


Figure P1.1-5

$0 = -v_{in} + R_1(i_a + i_b + i_c) + R_3(i_a)$

$$0 = -v_{in} + R_1(i_a + i_b + i_c) + R_2(i_b + i_c) + v_{out}$$

$$i_c = \frac{v_{out}}{R_4}$$

$$i_b = g_m v_1 = g_m i_a R_3$$

$$0 = -v_{in} + R_1\left(i_a + g_m i_a R_3 + \frac{v_{out}}{R_4}\right) + R_3 i_a$$

$$0 = -v_{in} + R_1\left(i_a + g_m i_a R_3 + \frac{v_{out}}{R_4}\right) + R_2\left(g_m i_a R_3 + \frac{v_{out}}{R_4}\right) + v_{out}$$

$$v_{in} = i_a (R_1 + R_3 + g_m R_1 R_2) + v_{out}\frac{R_1}{R_4}$$

$$v_{in} = i_a (R_1 + g_m R_1 R_3 + g_m R_2 R_3) + v_{out}\left(\frac{R_1 + R_2 + R_4}{R_4}\right)$$

$$v_{out} = \frac{\begin{vmatrix} R_1+R_3 + g_m R_1 R_3 & v_{in} \\ R_1+ g_m R_1 R_3 + g_m R_2 R_3 & v_{in} \end{vmatrix}}{\begin{vmatrix} R_1+ R_3 + g_m R_1 R_3 & R_1/ R_4 \\ R_1+ g_m R_1 R_3 + g_m R_2 R_3 & (R_1+ R_2+R_4) / R_4 \end{vmatrix}}$$

$$v_{out} = \frac{v_{in} R_3 R_4 (1 - g_m R_2)}{(R_1 + R_3 + g_m R_1 R_3)(R_1 + R_2 + R_4) - (R_1^2 + g_m R_1^2 R_3 + g_m R_1 R_2 R_3)}$$

$$v_{out} = \frac{v_{in} R_3 R_4 (1 - g_m R_2)}{R_1R_2 + R_1R_4 + R_1R_3 + R_2R_3 + R_3R_4 + g_m R_1 R_3 R_4}$$

$$\frac{v_{out}}{v_{in}} = \frac{R_3 R_4 (1 - g_m R_2)}{R_1R_2 + R_1R_4 + R_1R_3 + R_2R_3 + R_3R_4 + g_m R_1 R_3 R_4}$$

1.1-6 Use the source rearrangement and substitution concepts to simplify the circuit shown in Fig. P1.6 and solve for i_{out}/i_{in} by making chain-type calculations only.

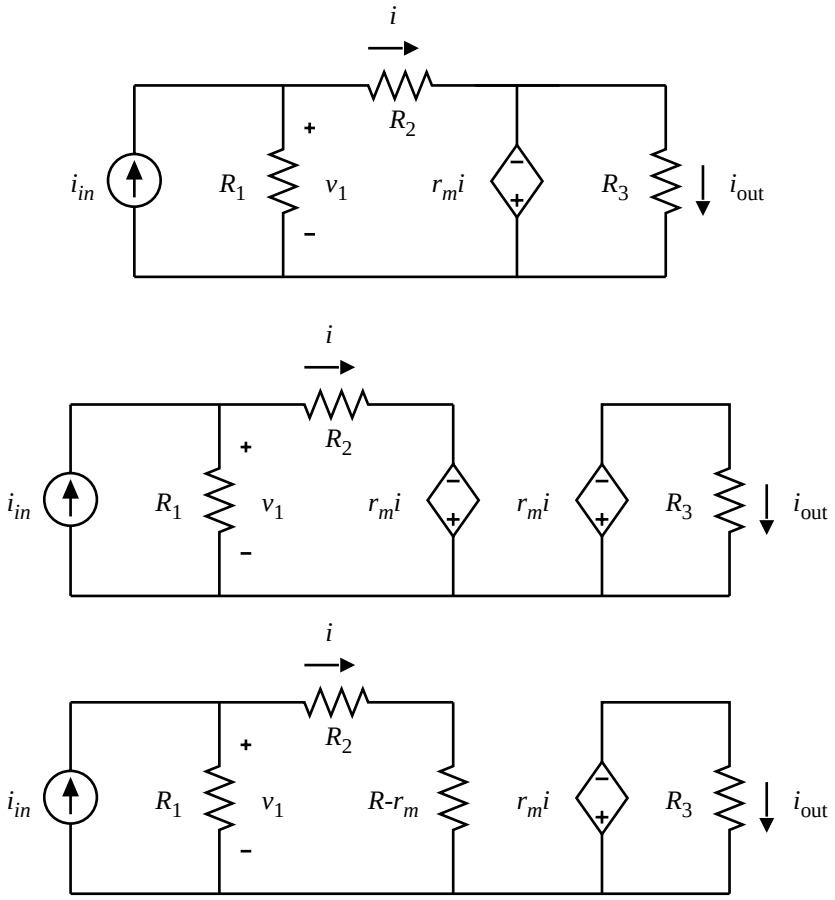


Figure P1.1-6

$$i_{\text{out}} = \frac{-r_m}{R_3} i$$

$$i = \frac{R_1}{R + R_1 - r_m} i_{\text{in}}$$

$$\frac{i_{\text{out}}}{i_{\text{in}}} = \frac{-r_m R_1/R_3}{R + R_1 - r_m}$$

1.1-7 Find v_2/v_1 and v_1/i_1 of Fig. P1.7.

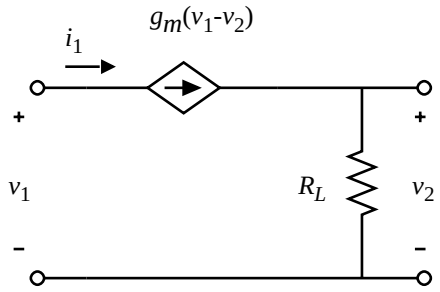


Figure P1.1-7

$$\frac{v_2}{v_1} = g_m\,(v_1 - v_2)\,R_L$$

$$v_2\,(1 + g_m\,R_L\,) = g_m\,R_L\,v_1$$

$$\frac{v_2}{v_1} = \frac{g_m\,R_L}{1 + g_m\,R_L}$$

$$v_2 = i_1\,R_L$$

substituting for v_2 yields:

$$\frac{i_1\,R_L}{v_1} = \frac{g_m\,R_L}{1 + g_m\,R_L}$$

$$\frac{v_1}{i_1} = \frac{R_L(\,1 + g_m\,R_L\,)}{g_m\,R_L}$$

$$\frac{v_1}{i_1} = R_L + \frac{1}{g_m}$$

1.1-8 Use the circuit-reduction technique to solve for v_{out}/v_{in} of Fig. P1.8.

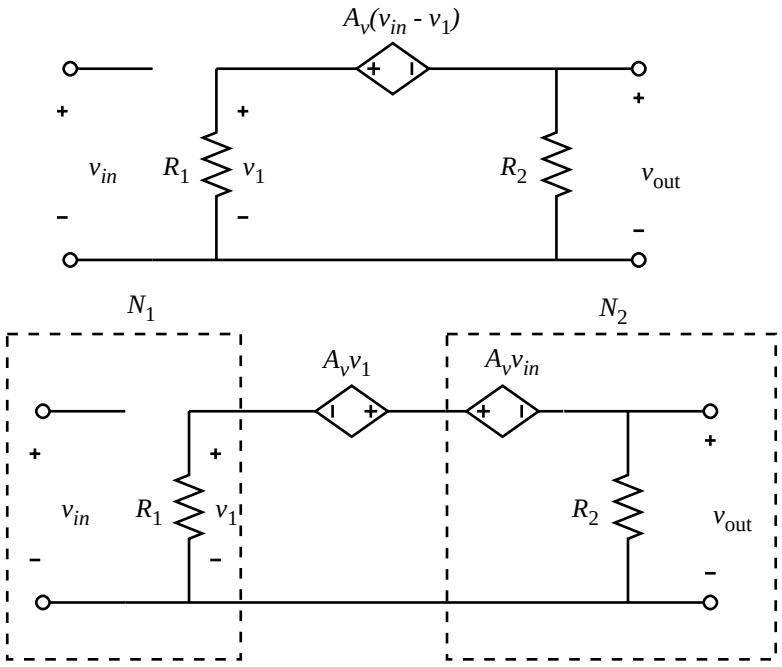


Figure P1.1-8a

Multiply R_1 by (A_v + 1)

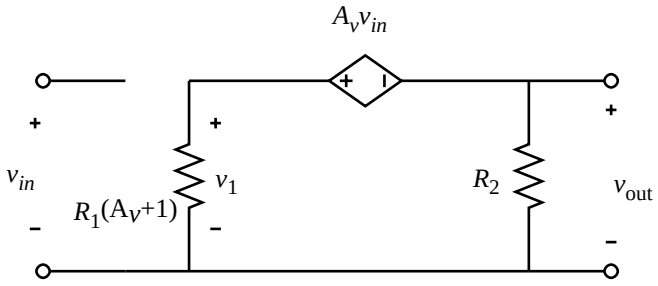


Figure P1.1-8b

$$v_{out} = \frac{-A_v v_{in} R_2}{R_2 + R_1(A_v+1)}$$

$$\frac{v_{out}}{v_{in}} = \frac{-A_v R_2}{R_2 + R_1(A_v+1)}$$

$$\frac{v_{out}}{v_{in}} = \frac{\frac{-A_v}{-A_v + 1} R_2}{\frac{R_2}{A_v + 1} + R_1}$$

As A_v approaches infinity,

$$\frac{v_{out}}{v_{in}} = \frac{-R_2}{R_1}$$

1.1-9 Use the Miller simplification concept to solve for v_{out}/v_{in} of Fig. A-3 (see Appendix A).

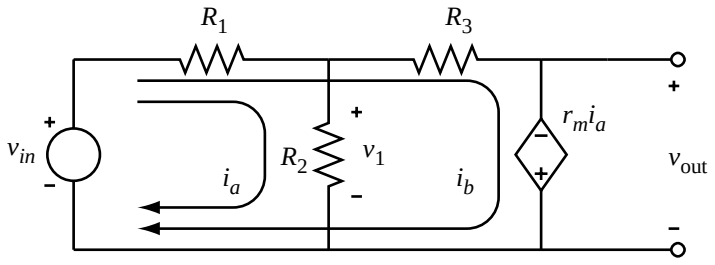


Figure P1.1-9a (Figure A-3 Mesh analysis.)

$$K = \frac{v_{out}}{v_1} = \frac{-r_m i_a}{i_a R_2} = \frac{-r_m}{R_2}$$

$$Z_1 = \frac{R_3}{1 + \frac{r_m}{R_2}}$$

$$Z_2 = \frac{R_3 \frac{-r_m}{R_2}}{-\frac{r_m}{R_2} - 1}$$

$$Z_2 = \frac{r_m \frac{R_3}{R_2}}{\frac{r_m}{R_2} + 1} = \frac{R_3}{\frac{R_2}{r_m} + 1}$$

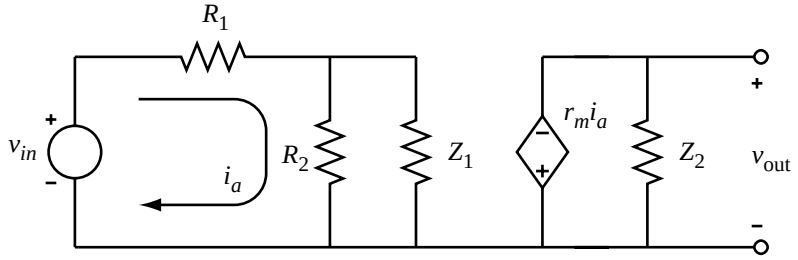


Figure P1.1-9b

$$i_a = \frac{v_{in}\,(R_2 \parallel Z_1)}{(R_2 \parallel Z_1) + R_1}\left(\frac{1}{R_2}\right)$$

$$v_{out} = -r_m\, i_a$$

$$v_{out} = \frac{-v_{in}\, r_m\,(R_2 \parallel Z_1)}{(R_2 \parallel Z_1) + R_1}\left(\frac{1}{R_2}\right)$$

$$\frac{v_{out}}{v_{in}} = \frac{-r_m\,(R_2 \parallel Z_1)}{(R_2 \parallel Z_1) + R_1}\left(\frac{1}{R_2}\right)$$

$$\frac{v_{out}}{v_{in}} = \frac{-r_m\, R_3}{(R_1R_2 + R_1R_3 + R_1r_m + R_2R_3)}$$

1.1-10 Find v_{out}/i_{in} of Fig. A-12 and compare with the results of Example A-1.

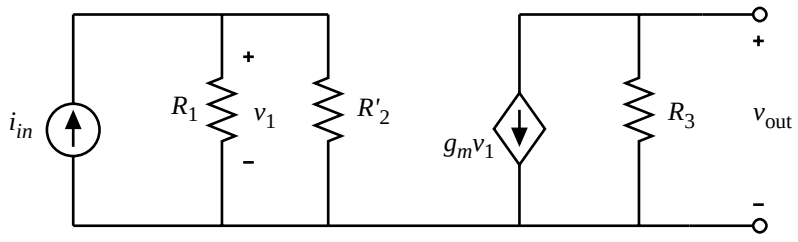


Figure P1.1-10

$$v_1 = i_{in}\,(R_1 \parallel R_2')$$

$$v_{out} = -g_m v_1 R_3 = -g_m R_3\, i_{in}\,(R_1 \parallel R_2')$$

$$\frac{v_{out}}{i_{in}} = -g_m R_3 (R_1 \parallel R_2')$$

$$R_2' = \frac{R_2}{1 + g_m R_3}$$

$$R_1 \parallel R_2' = \frac{\dfrac{R_1 R_2}{1 + g_m R_3}}{\dfrac{(1 + g_m R_3) R_1 + R_2}{1 + g_m R_3}}$$

$$R_1 \parallel R_2' = \frac{R_1 R_2}{(1 + g_m R_3) R_1 + R_2}$$

$$\frac{v_{out}}{i_{in}} = \frac{-g_m R_1 R_2 R_3}{R_1 + R_2 + R_3 + g_m R_1 R_3}$$

The A.1-1 result is:

$$\frac{v_{out}}{i_{in}} = \frac{R_1 R_3 - g_m R_1 R_2 R_3}{R_1 + R_2 + R_3 + g_m R_1 R_3}$$

if $g_m R_2 >> 1$ then the results are the same.

1.1-11 Use the Miller simplification technique described in Appendix A to solve for the output resistance, v_o/i_o, of Fig. P1.4. Calculate the output resistance not using the Miller simplification and compare your results.

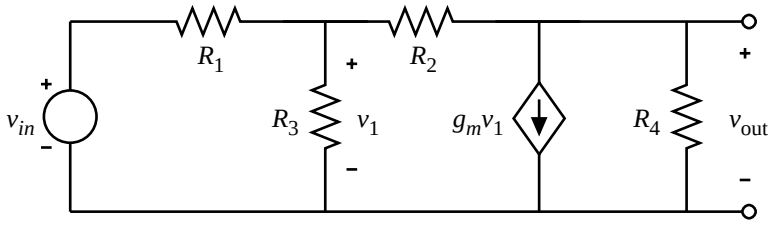


Figure P1.1-11a

Z_o with Miller

$K = -g_m R_4$

$$Z_2 = \frac{-R_2 g_m R_4}{-g_m R_4 - 1} = \frac{R_2 g_m R_4}{1 + g_m R_4}$$

$$Z_0 = R_4 \parallel Z_2 = \frac{\frac{g_m R_2 R_4^2}{1 + g_m R_4}}{\frac{(1 + g_m R_4) R_4 + g_m R_2 R_4^2}{1 + g_m R_4}}$$

$$Z_0 = R_4 \parallel Z_2 = \frac{g_m R_2 R_4^2}{R_4 + g_m R_4 (R_4 + R_2)}$$

Z_o without Miller

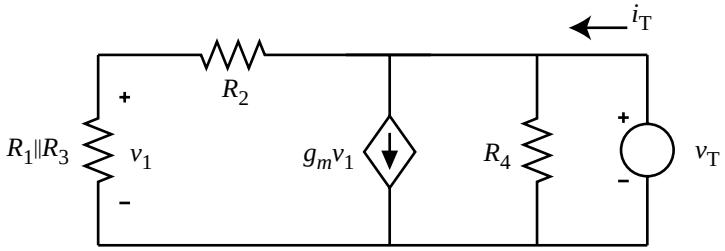


Figure P1.1-11b

$$v_1 = (R_1 \parallel R_3)\left(i + g_m v_1 - \frac{v_T}{R_4}\right)$$

$$v_1 [1 + g_m (R_1 \parallel R_3)] = (R_1 \parallel R_3)\left(i_T + - \frac{v_T}{R_4}\right)$$

$$(1) \quad v_1 = \frac{(R_1 \parallel R_3)(i_T R_4 + - v_T)}{R_4 [1 + g_m (R_1 \parallel R_3)]}$$

$$(2) \quad v_1 = \frac{v_T\,(R_1 \parallel R_3)}{R_1 \parallel R_3 + R_2}$$

Equate (1) and (2)

$$\frac{v_T\ (R_1 \parallel R_3)}{R_1 \parallel R_3 + R_2} = \frac{(R_1 \parallel R_3)\,(i_T R_4 - v_T)}{R_4\,[1 + g_m\,(R_1 \parallel R_3)]}$$

$$\frac{v_T}{R_1 \parallel R_3 + R_2} = \frac{i_T R_4 - v_T}{R_4\,[1 + g_m\,(R_1 \parallel R_3)]}$$

$$v_T \left\{ R_4\,[1 + g_m\,(R_1 \parallel R_3)] + R_2 + R_1 \| R_3 \right\} = i_T R_4\,(R_2 + R_1 \| R_3)$$

$$Z_0 = \frac{R_4\,(R_2 + R_1 \| R_3\,)}{R_2 + R_4 + g_m R_4 (R_1 \| R_3) + R_1 \| R_3}$$

$$Z_0 = \frac{R_4 R_2 + \dfrac{R_1 R_3 R_4}{R_1 + R_3}}{R_2 + R_4 + \dfrac{g_m R_4 R_1 R_3 + R_1 R_3}{R_1 + R_3}}$$

$$Z_0 = \frac{R_4 R_2\,(R_1 + R_3) + R_1 R_3 R_4}{(R_2 + R_4)\,(R_1 + R_3) + R_1 R_3 + g_m R_1 R_3 R_4}$$

$$Z_0 = \frac{R_1 R_2 R_4 + R_2 R_3 R_4 + R_1 R_3 R_4}{R_1 R_2 + R_2 R_3 + R_3 R_4 + R_1 R_4 + R_1 R_3 + g_m R_1 R_3 R_4}$$

1.1-12 Consider an ideal voltage amplifier with a voltage gain of $A_v = 0.99$. A resistance R = 50 kΩ is connected from the output back to the input. Find the input resistance of this circuit by applying the Miller simplification concept.

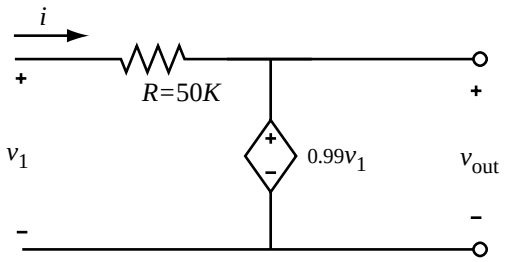


Figure P1.1-12

$$R_{in} = \frac{R}{1 - K}$$

$K = 0.99$

$$R_{in} = \frac{50\ K\Omega}{1 - 0.99} = \frac{50\ K\ \Omega}{0.01} = 5\ \text{Meg}\ \Omega$$

Chapter 2 Homework Solutions

Problem 2.1-1
List the five basic MOS fabrication processing steps and give the purpose or function of each step.

Oxidation: Combining oxygen and silicon to form silicondioxide (SiO_2). Resulting SiO_2 formed by oxidation is used as an isolation barrier (e.g., between gate polysilicon and the underlying channel) and as a dielectric (e.g., between two plates of a capacitor).

Diffusion: Movement of impurity atoms from one location to another (e.g., from the silicon surface to the bulk to form a diffused well region).

Ion Implantation: Firing ions into an undoped region for the purpose of doping it to a desired concentration level. Specific doping profiles are achievable with ion implantation which cannot be achieved by diffusion alone.

Deposition: Depositing various films on to the wafer. Used to deposit dielectrics which cannot be grown because of the type of underlying material. Deposition methods are used to lay down polysilicon, metal, and the dielectric between them.

Etching: Removal of material sensitive to the etch process. For example, etching is used to eliminate unwanted polysilicon after it has been laid out by deposition.

Problem 2.1-2
What is the difference between positive and negative photoresist and how is photoresist used?

Positive: Exposed resist changes chemically so that it can dissolve upon exposure to light. Unexposed regions remain intact.

Negative: Unexposed resist changes chemically so that it can dissolve upon exposure to light. Exposed regions remain intact.

Photoresist is used as a masking layer which is paterned appropriately so that certain underlying regions are exposed to the etching process while those regions covered by photoresist are resistant to etching.

Problem 2.1-3
Illustrate the impact on source and drain diffusions of a 7° angle off perpendicular ion implant. Assume that the thickness of polysilicon is 8000 Å and that out diffusion from point of ion impact is 0.07 μm.

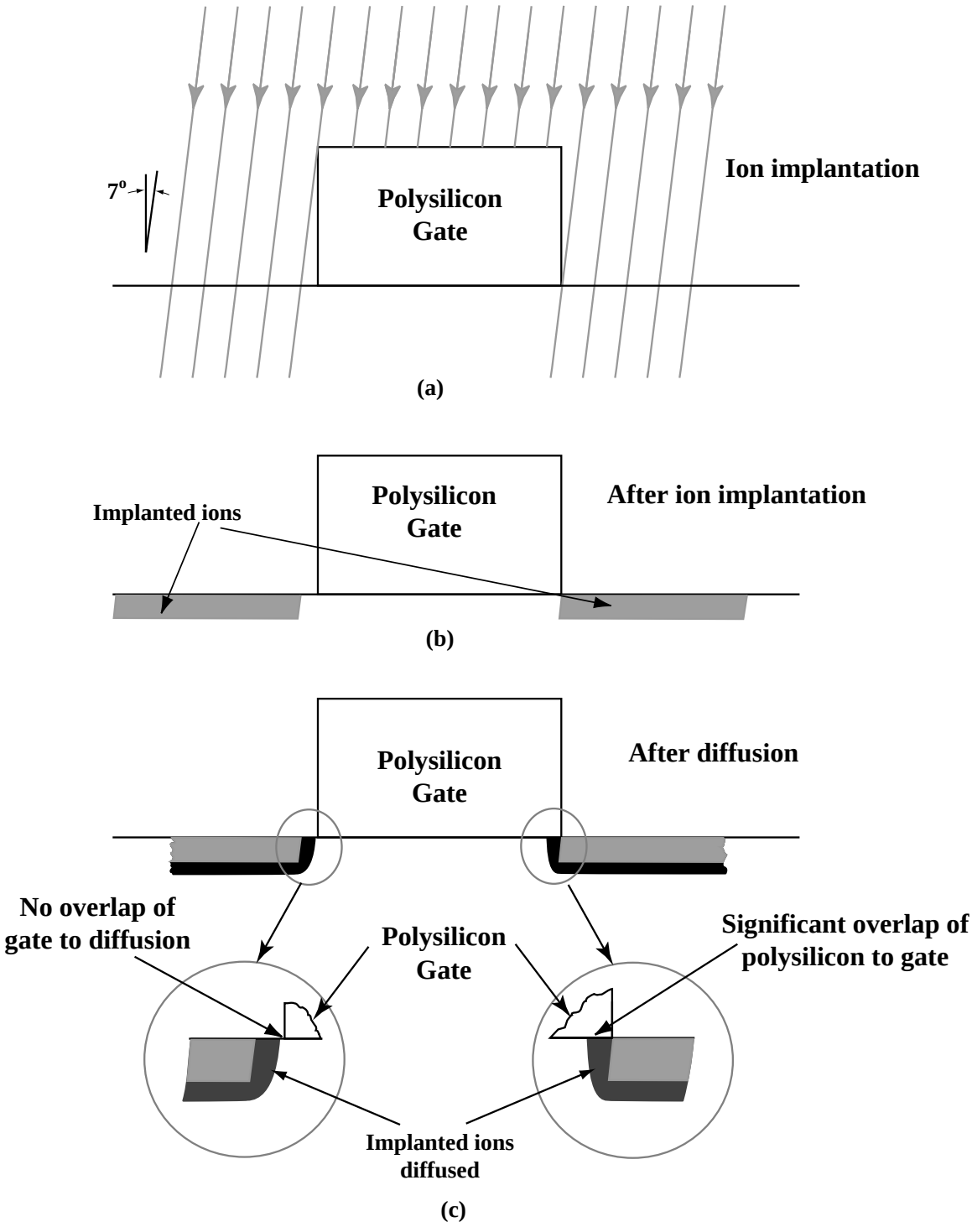


Figure P2.1-3

Problem 2.1-4

What is the function of silicon nitride in the CMOS fabrication process described in Section 2.1

The primary purpose of silicon nitride is to provide a barrier to oxygen so that when deposited and patterned on top of silicon, silicon dioxide does not form below where the silicon nitride exists.

Problem 2.1-5
Give typical thickness for the field oxide (FOX), thin oxide (TOX), n^+ or p^+, p-well, and metal 1 in units of μm.
FOX: ~ 1 μm
TOX: ~ 0.014 μm for an 0.8 μm process
N+/p+: ~ 0.2 μm
Well: ~ 1.2 μm
Metal 1: ~ 0.5 μm

Problem 2.2-1
Repeat Example 2.2-1 if the applied voltage is -2 V.

$N_A = 5 \times 10^{15}/\text{cm}^3$, $N_D = 10^{20}/\text{cm}^3$

$$\phi_o = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) = \frac{1.381\times10^{-23}\times300}{1.6\times10^{-19}} \ln\left(\frac{5\times10^{15}\times10^{20}}{(1.45\times10^{10})^2}\right) = 0.9168$$

$$x_n = \left[\frac{2\varepsilon_{si}(\phi_o - v_D)N_A}{qN_D(N_A + N_D)}\right]^{1/2} = \left[\frac{2\times11.7\times8.854\times10^{-14}\,(0.9168 + 2.0)\,5\times10^{15}}{1.6\times10^{-19}\times10^{20}\,(5\times10^{15} + 10^{20})}\right]^{1/2} = 43.5\times10^{-12}\ \text{m}$$

$$x_p = -\left[\frac{2\varepsilon_{si}(\phi_o - v_D)N_D}{qN_A(N_A + N_D)}\right]^{1/2} = \left[\frac{2\times11.7\times8.854\times10^{-14}\,(0.9168 + 2.0)\,10^{20}}{1.6\times10^{-19}\times5\times10^{15}\,(5\times10^{15} + 10^{20})}\right]^{1/2} = -0.869\ \mu\text{m}$$

$$x_d = x_n - x_p = 0 + 0.869\ \mu\text{m} = 0.869\ \mu\text{m}$$

$$C_{j0} = \frac{dQ_j}{dv_D} = A\left[\frac{\varepsilon_{si} q N_A N_D}{2(N_A + N_D)\,(\phi_o)}\right]^{1/2}$$

$$C_{j0} = 1\times10^{-3}\times1\times10^{-3}\left[\frac{11.7\times8.854\times10^{-14}\times1.6\times10^{-19}\times5\times10^{15}\times1\times10^{20}}{2(5\times10^{15}+1\times10^{20})\,(0.917)}\right]^{1/2} = 21.3\ \text{fF}$$

$$C_{j0} = \frac{C_{j0}}{\left(1 - \frac{\phi_0}{v_D}\right)^{1/2}} = \frac{21.3 \text{ fF}}{\left(1 - \frac{-2}{0.917}\right)^{1/2}} = 11.94 \text{ fF}$$

Problem 2.2-2
Develop Eq. (2.2-9) using Eqs. (2.2-1), (2.2-7), and (2.2-8).

Eq. 2.2-1

$$x_d = x_n - x_p$$

Eq. 2.2-7

$$x_n = \left[\frac{2\varepsilon_{si}(\phi_o - v_D)N_A}{qN_D(N_A + N_D)}\right]^{1/2}$$

Eq. 2.2-8

$$x_p = -\left[\frac{2\varepsilon_{si}(\phi_o - v_D)N_D}{qN_A(N_A + N_D)}\right]^{1/2}$$

$$x_d = \left[\frac{2\varepsilon_{si}(\phi_o - v_D)N_A^2 + 2\varepsilon_{si}(\phi_o - v_D)N_D^2}{qN_A N_D (N_A + N_D)}\right]^{1/2}$$

$$x_d = (\phi_o - v_D)^{1/2}\left[\frac{2\varepsilon_{si}\left(N_A^2 + N_D^2\right)}{qN_A N_D (N_A + N_D)}\right]^{1/2}$$

Assuming that $2N_A N_D << (N_A + N_D)^2$

Then

$$x_d = (\phi_o - v_D)^{1/2}\left[\frac{2\varepsilon_{si}(N_A + N_D)^2}{qN_A N_D (N_A + N_D)}\right]^{1/2}$$

$$x_d = (\phi_o - v_D)^{1/2}\left[\frac{2\varepsilon_{si}(N_A + N_D)}{qN_A N_D}\right]^{1/2}$$

Problem 2.2-3
Redevelop Eqs. (2.2-7) and (2.2-8) if the impurity concentration of a pn junction is given by Fig. 2.2-2 rather than the step junction of Fig. 2.2-1(b).

Referring to Figure P2.2-3

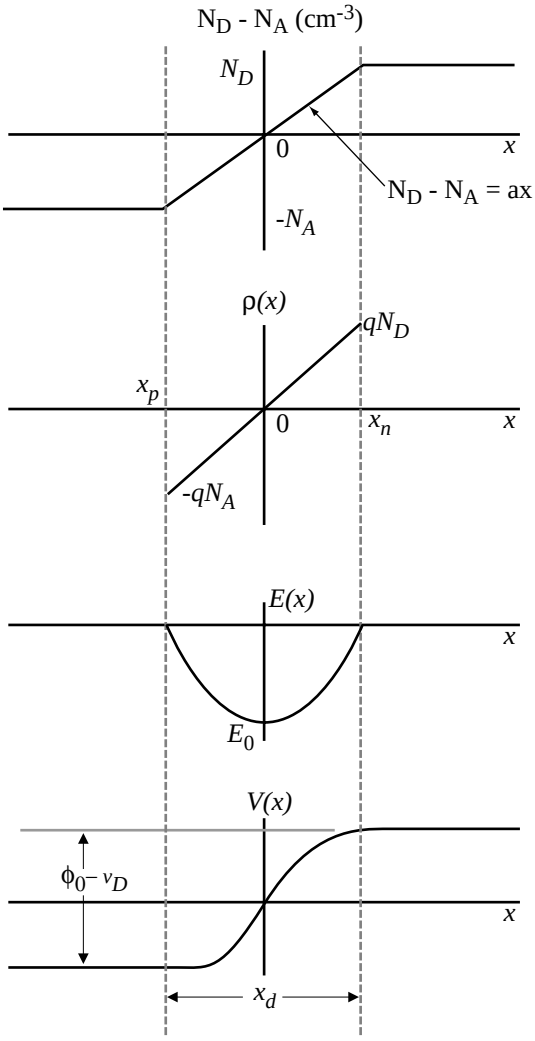


Figure P2.2-3

Using Poisson's equation in one dimension

$$\frac{d^2V}{dx^2} = -\frac{\rho(x)}{\varepsilon}$$

$$\rho(x) = qax \;, \quad when \quad x_p < x < x_n$$

$$\frac{d^2V}{dx^2} = -\frac{qax}{\varepsilon}$$

$$E(x) = -\frac{dV}{dx} = \frac{qa}{2\varepsilon}x^2 + C_1$$

$$E(x_p) = E(x_n) = 0$$

then

$$0 = \frac{qa}{2\varepsilon} x_p^2 + C_1$$

$$C_1 = -\frac{qa}{2\varepsilon} x_p^2$$

$$E(x) = \frac{qa}{2\varepsilon} x^2 - \frac{qa}{2\varepsilon} x_p^2 = \frac{qa}{2\varepsilon}\left(x^2 - x_p^2\right)$$

The voltage across the junction is given as

$$V = -\int_{x_p}^{x_n} E(x)dx = -\frac{qa}{2\varepsilon}\int_{x_p}^{x_n}\left(x^2 - x_p^2\right)dx$$

$$V = -\frac{qa}{2\varepsilon}\left(\frac{x^3}{3} - x_p^2 x\right)\Bigg|_{x_p}^{x_n}$$

$$V = -\frac{qa}{2\varepsilon}\left[\left(\frac{x_n^3}{3} - x_p^2 x_n\right) - \left(\frac{x_p^3}{3} - x_p^2 x_p\right)\right]$$

$$V = -\frac{qa}{2\varepsilon}\left[\left(\frac{x_n^3}{3} - x_p^2 x_n\right) - x_p^3\left(\frac{1}{3} - 1\right)\right] = -\frac{qa}{2\varepsilon}\left[\frac{x_n^3}{3} - x_p^2 x_n + \frac{2}{3}x_p^3\right]$$

Since $-x_p = x_n$

$$V = -\frac{qa}{2\varepsilon}\left[-\frac{x_p^3}{3} + x_p^3 + \frac{2}{3}x_p^3\right] = -\frac{qa}{2\varepsilon}x_p^3\left[-\frac{1}{3} + 1 + \frac{2}{3}\right] = -\frac{qa}{2\varepsilon}x_p^3\left(\frac{4}{3}\right)$$

$$V = -\frac{2qa}{3\varepsilon}x_p^3$$

V represents the barrier potential across the junction, $\phi_0 - V_D$. Therefore

$$\phi_0 - V_D = \frac{2qa}{3\varepsilon} x_p^3$$

$$x_p = -x_n = \left(\frac{3\varepsilon}{2qa}\right)^{1/3} (\phi_0 - V_D)^{1/3}$$

Problem 2.2-4

Plot the normalized reverse current, i_{RA}/i_R, versus the reverse voltage v_R of a silicon pn diode which has $BV = 12$ V and $n = 6$.

$$\frac{i_{RA}}{i_R} = \left[\frac{1}{1 - (v_R/BV)^n}\right]$$

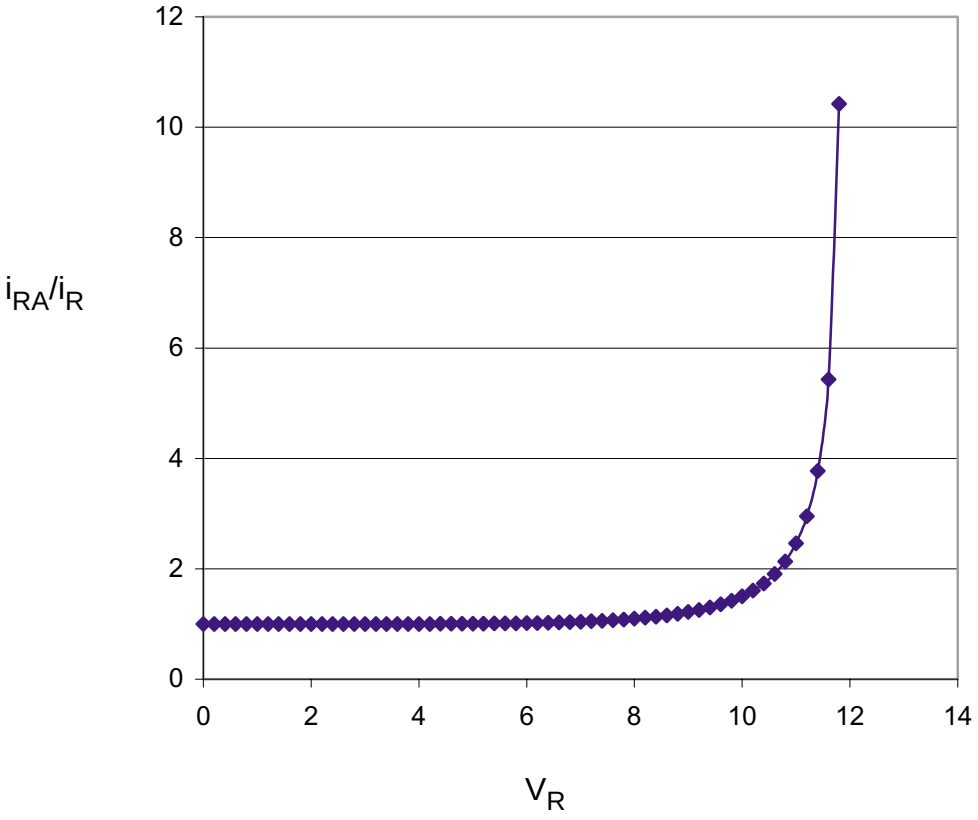


Figure P2.2-4

Problem 2.2-5

What is the breakdown voltage of a pn junction with $N_A = N_D = 10^{16}/\text{cm}^3$?

$$BV \cong \frac{\varepsilon_{si}(N_A + N_D)}{2qN_AN_D} E_{\max}^2$$

$$BV \cong \frac{11.7\times8.854\times10^{-14}\,(10^{16} + 10^{16})}{2\times1.6\times10^{-19}\times10^{16}\times10^{16}} (3\times10^5)^2 = 58.27 \text{ volts}$$

Problem 2.2-6
What change in v_D of a silicon pn diode will cause an increase of 10 (an order of magnitude) in the forward diode current?

$$i_D = I_s\left[\exp\left(\frac{v_D}{V_t}\right) - 1\right] \cong I_s \exp\left(\frac{v_D}{V_t}\right)$$

$$\frac{10\, i_D}{i_D} = \frac{I_s \exp\left(\frac{v_{D1}}{V_t}\right)}{I_s \exp\left(\frac{v_{D2}}{V_t}\right)} = \frac{\exp\left(\frac{v_{D1}}{V_t}\right)}{\exp\left(\frac{v_{D2}}{V_t}\right)} = \exp\left(\frac{v_{D1} - v_{D2}}{V_t}\right)$$

$$10 = \exp\left(\frac{v_{D1} - v_{D2}}{V_t}\right)$$

$$V_t \ln(10) = v_{D1} - v_{D2}$$

$$25.9 \text{ mV} \times 2.303 = 59.6 \text{ mV} = v_{D1} - v_{D2}$$

$$v_{D1} - v_{D2} = 59.6 \text{ mV}$$

Problem 2.3-1
Explain in your own words why the magnitude of the threshold voltage in Eq. (2.3-19) increases as the magnitude of the source-bulk voltage increases (The source-bulk pn diode remains reversed biased.)

Considering an n-channel device, as the gate voltage increases relative to the bulk, the region under the gate will begin to invert. What happens near the source? If the source is at the same potential as the bulk, then the region adjacent to the edge of the source inverts as the rest of the bulk region under the gate inverts. However, if the source is at a higher potential than the bulk, then a greater gate voltage is required to overcome the electric field induced by the source. While a portion of the region under the gate still inverts, there is no path of current flow to the source because the gate voltage is not large enough to invert right at the source edge. Once

the gate is greater than the source and increasing, then the region adjacent to the source can begin to invert and thus provide a current path into the channel.

Problem 2.3-2
If $V_{SB} = 2$ V, find the value of V_T for the n-channel transistor of Ex. 2.3-1.

$2\phi_F = -0.940$
$\gamma = 0.577$
$V_{T0} = 0.306$

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + v_{SB}|} - \sqrt{|-2\phi_F|})$$

$$V_T = 0.306 + 0.577\ (\sqrt{|0.940 + 2|} - \sqrt{|0.940|}) = 0.736 \text{ volts}$$

$V_T = 0.736$ volts

Problem 2.3-3
Re-derive Eq. (2.3-27) given that V_T is not constant in Eq. (2.3-22) but rather varies linearly with $v(y)$ according to the following equation.

$V_T = V_{T0} + a\ \ v(y)$ << correction to book

$$\int_0^L i_D\, dy = \int_0^{v_{DS}} W\mu_n Q_I(y)\ dv(y) = \int_0^{v_{DS}} W\mu_n C_{ox}[v_{GS} - v(y) - V_{T(y)}]\, dv(y)$$

$$V_{T(y)} = V_{T0} + a\, v(y)$$

$$i_D L = \int_0^{v_{DS}} W\mu_n C_{ox}[v_{GS} - v(y) - V_{T0} - a\, v(y)]\, dv(y)$$

$$i_D L = W\mu_n C_{ox} \int_0^{v_{DS}} [v_{GS} - V_{T0} - v(y)\,(1 + a)]\, dv(y)$$

$$i_D L = W\mu_n C_{ox} \left[(v_{GS} - V_{T0})v(y) - (1 + a)\frac{v(y)^2}{2} \right]_0^{v_{DS}}$$

$$i_D = \frac{W\mu_n C_{ox}}{\mathrm{L}}\left[(v_{GS} - V_{T0})\, v_{DS} - (1 + a)\frac{v_{DS}^{\ 2}}{2} \right]$$

Problem 2.3-4
If the mobility of an electron is 500 $cm^2/(V{\cdot}s)$ and the mobility of a hole is 200 $cm^2/(V{\cdot}s)$, compare the performance of an n-channel with a p-channel transistor. In particular, consider the value of the transconductance parameter and speed of the MOS transistor.

Since $K' = \mu C_{ox}$, the transconductance of an n-channel transistor will be 2.5 time greater than the transconductance of a p-channel transistor. Remember that mobility will degrade as a function of terminal conditions so transconductance will degrade as well. The speed of a circuit is determined in a large part by the capacitance at the terminals and the transconductance. When terminal capacitances are equal for an n-channel and p-channel transistor of the same dimensions, the higher transconductance of the n-channel results in a faster circuit.

Problem 2.3-5
Using Ex. 2.3-1 as a starting point, calculate the difference in threshold voltage between two devices whose gate-oxide is different by 5% (i.e., $t_{ox} = 210$ Å).

$$\phi_F(\text{substrate}) = -0.0259 \ln\left[\frac{3\times 10^{16}}{1.45\times 10^{10}}\right] = -0.377 \text{ V}$$

$$\phi_F(\text{gate}) = 0.0259 \ln\left[\frac{4\times 10^{19}}{1.45\times 10^{10}}\right] = 0.563 \text{ V}$$

$$\phi_{MS} = \phi_F(\text{substrate}) - \phi_F(\text{gate}) = -0.940 \text{ V}.$$

$$C_{ox} = \varepsilon_{ox}/t_{ox} = \frac{3.9\times 8.854\times 10^{-14}}{210\times 10^{-8}} = 1.644\times 10^{-7} \text{ F/cm}^2$$

$$Q_{b0} = -\left(2\times 1.6\times 10^{-19}\times 11.7\times 8.854\times 10^{-14}\times 2\times 0.377\times 3\times 10^{16}\right)^{1/2}$$

$$= -8.66\times 10^{-8} \text{ C/cm}^2.$$

$$\frac{Q_{b0}}{C_{ox}} = \frac{-8.66 \times 10^{-8}}{1.644 \times 10^{-7}} = -0.5268 \text{ V}$$

$$\frac{Q_{ss}}{C_{ox}} = \frac{10^{10} \times 1.60 \times 10^{-19}}{1.644 \times 10^{-7}} = 9.73 \times 10^{-3} \text{ V}$$

$$V_{T0} = -0.940 + 0.754 + 0.5268 - 9.73 \times 10^{-3} = 0.331 \text{ V}$$

$$\gamma = \frac{\left[2 \times 1.6 \times 10^{-19} \times 11.7 \times 8.854 \times 10^{-14} \times 3 \times 10^{16}\right]^{1/2}}{1.644 \times 10^{-7}} = 0.607 \quad \text{V}^{1/2}$$

Problem 2.3-6
Repeat Ex. 2.3-1 using $N_A = 7 \times 10^{16}$ cm^{-3}, gate doping, $N_D = 1 \times 10^{19}$ cm^{-3}.

$$\phi_F(\text{substrate}) = -0.0259 \ln\left[\frac{7 \times 10^{16}}{1.45 \times 10^{10}}\right] = -0.3986 \text{ V}$$

$$\phi_F(\text{gate}) = 0.0259 \ln\left[\frac{1 \times 10^{19}}{1.45 \times 10^{10}}\right] = 0.527 \text{ V}$$

$$\phi_{MS} = \phi_F(\text{substrate}) - \phi_F(\text{gate}) = -0.9256 \text{ V}.$$

$$C_{ox} = \varepsilon_{ox}/t_{ox} = \frac{3.9 \times 8.854 \times 10^{-14}}{200 \times 10^{-8}} = 1.727 \times 10^{-7} \text{ F/cm}^2$$

$$Q_{b0} = -\left(2 \times 1.6 \times 10^{-19} \times 11.7 \times 8.854 \times 10^{-14} \times 2 \times 0.3986 \times 7 \times 10^{16}\right)^{1/2}$$

$$= -13.6 \times 10^{-8} \text{ C/cm}^2.$$

$$\frac{Q_{b0}}{C_{ox}} = \frac{-13.6 \times 10^{-8}}{1.727 \times 10^{-7}} = -0.7875 \text{ V}$$

$$\frac{Q_{ss}}{C_{ox}} = \frac{10^{10} \times 1.60 \times 10^{-19}}{1.727 \times 10^{-7}} = 9.3 \times 10^{-3} \text{ V}$$

$$V_{T0} = -0.9256 + 0.797 + 0.7875 - 9.3 \times 10^{-3} = 0.6496 \text{ V}$$

$$\gamma = \frac{\left[2 \times 1.6 \times 10^{-19} \times 11.7 \times 8.854 \times 10^{-14} \times 7 \times 10^{16}\right]^{1/2}}{1.727 \times 10^{-7}} = 0.882 \quad \text{V}^{1/2}$$

Problem 2.4-1
Given the component tolerances in Table 2.4-1, design the simple lowpass filter illustrated in Fig P2.4-1 to minimize the variation in pole frequency over all process variations. Pole frequency should be designed to a nominal value of 1MHz. You must choose the appropriate capacitor and resistor type. Explain your reasoning. Calculate the variation of pole frequency over process using the design you have chosen.

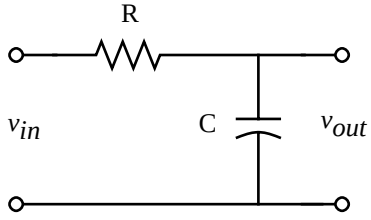


Figure P2.4.1

- To minimize distortion, we would choose minimum voltage coefficient for resistor and capacitor.

- To minimize variation, we choose components with the lowest tolerance.

The obvious choice for the resistor is Polysilicon. The obvious choice for the capacitor is the MOS capacitor. Thus we have the following:

We want $\omega_{-3dB} = 2\pi \times 10^6 = 1/RC$

C = 2.2 fF/μm^2 to 2.7 fF/μm^2 ; R = 20 Ω/❑ to 40 Ω/❑

Nominal values are
C = 2.45 fF/μm^2 ; R = 30 Ω/❑

In order to minimize total area used, you can do the following:

Set resistor width to 5μm (choosing a different width is OK).
Define:

N = the number of squares for the resistor
A_C = area for the capacitor.

Then:

$R = N \times 30$
$C = A_C \times C'$ (use C' to avoid confusion)

We want:

$$RC = \frac{1}{2\pi \times 10^6}$$

Total area = $A_{tot} = N \times 25 + A_C$

$$A_{tot} = 25 \times N + \frac{1.59 \times 10^6}{N}$$

To minimize area, set

$$\frac{\partial A_{tot}}{\partial N} = 25 - \frac{1.59 \times 10^6}{N^2} = 0$$

$N = 252 \Rightarrow A_C = 6308\ \mu m^2$

Nominal values for R and C:

$R = 7.56\ k\Omega$; $C = 15.45$ pF

Minimum values for R and C:

$R = 5.04\ k\Omega$; $C = 13.88$ pF

Maximum values for R and C:

$R = 10.08\ k\Omega$; $C = 17.03$ pF

$$\text{Max pole frequency} = \frac{1}{(2\pi)(5.04k)\ (13.88pF)} \Rightarrow 2.275\ \text{MHz}$$

$$\text{Min pole frequency} = \frac{1}{(2\pi)(10.08k)\ (17.03pF)} \Rightarrow 927\ \text{kHz}$$

Problem 2.4-2

List two sources of error that can make the actual capacitor, fabricated using a CMOS process, differ from its designed value.

Sources of error are:

- Variations in oxide thickness between the capacitor plates
- Dimensional variations of the plates due to the tolerance in
  - Etch
  - Mask
- Registration error (between layers)

Problem 2.4-3
What is the purpose of the n^+ implantation in the capacitor of Fig. 2.4-1(a)?

The implant is required to form a diffusion with a doping similar to that of the drain and source. As the voltage across the capacitor varies, depleting the bottom plate of carriers causes the capacitor to have a voltage coefficient which can have a bad effect on analog performance. With a highly-doped diffusion below the top plate, voltage coefficient is minimized.

Problem 2.4-4
Consider the circuit in Fig. P2.4-4. Resistor R_1 is an n-well resistor with a nominal value of 10 kΩ when the voltage at both terminals is 3 V. The input voltage, v_{in}, is a sine wave with an amplitude of 2 VPP and a dc component of 3 V. Under these conditions, the value of R_1 is given as

$$R_1 = R_{nom}\left[1 + K\left(\frac{v_{in} + v_{out}}{2}\right)\right]$$

where R_{nom} is 10K and the coefficient K is the voltage coefficient of an n-well resistor and has a value of 10K ppm/V. Resistor R_2 is an ideal resistor with a value of 10 kΩ. Derive a time-domain expression for v_{out}. Assume that there are no frequency dependencies.

TBD

Problem 2.4-5
Repeat problem 21 using a P+ diffused resistor for R_1. Assume that a P+ resistor's voltage coefficient is 200 ppm/V. The n-well in which R1 lies, is tied to a 5 volt supply.

TBD

Problem 2.4-6
Consider problem 2.4-5 again but assume that the n-well in which R1 lies is not connected to a 5 volt supply, but rather is connected as shown in Fig. P2.4-6.

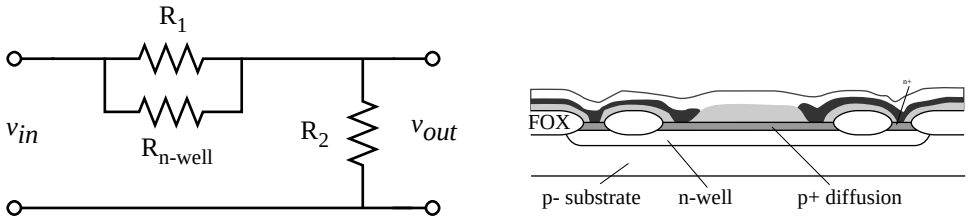
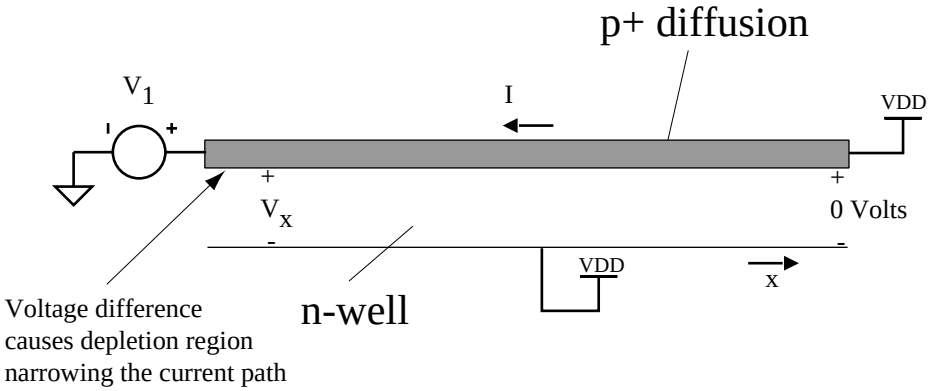
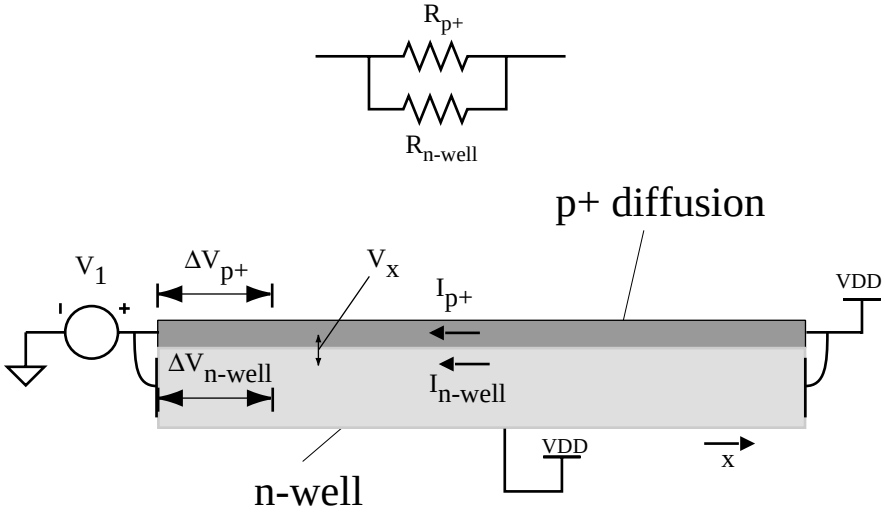


Figure P2.4-6

Voltage effects a resistor's value when the voltage between any point along the current path in the resistor and the material in which it lies. The voltage difference causes a depletion region to form in the resistor, thus increasing its resistance. This idea is illustrated in the diagram below.



In order to keep the depletion region from varying along the direction of the current path, the potential of the material below the p+ diffusion (n-well in this case) must vary in the same way as the potential of the p+ diffusion. This is accomplished by causing current to flow in the underlying material (n-well) in parallel with the current in the p+ diffusion as illustrated below.



It is easy to see that if $\Delta V_{p+} = \Delta V_{n\text{-}well}$ then $V_x = 0$. Thus by attaching the n-well in parallel with the desired current path, the effects of voltage coefficient of the p+ material are eliminated. There is a second-order effect due to the fact that the n-well resistor will have a voltage coefficient due to the underlying material (p- substrate) tied to ground. Even with this non-ideal effect, significant improvement is achieved by this method.

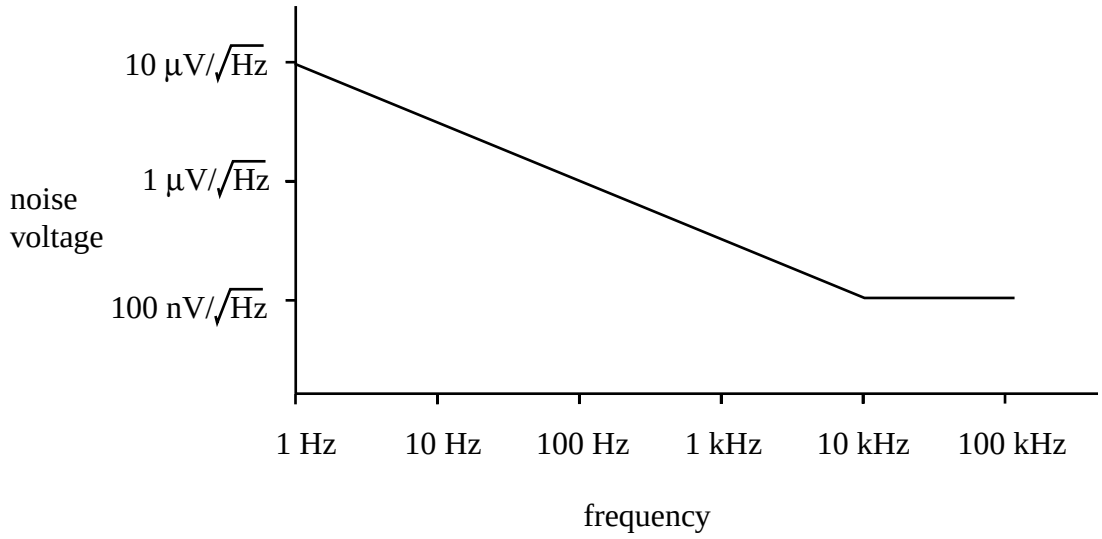
Problem 2.5-1
Assume $v_D = 0.7$ V and find the fractional temperature coefficient of I_s and v_D.

$$\frac{1}{I_S}\frac{dI_S}{dT} = \frac{3}{T} + \frac{1}{T}\frac{V_{Go}}{V_t} = \frac{3}{300} + \frac{1}{300}\ \frac{1.205}{0.0259} = 0.1651$$

$$\frac{dv_D}{dT} = -\left[\frac{V_{Go}\ 1.942\times 10^{-3}\ v_D}{T}\right] - \frac{3V_t}{T} = -\left[\frac{1.205 - 0.7}{300}\right] - \frac{3\times 0.0259}{300} = 1.942\times 10^{-3}$$

$$\frac{1}{v_D}\frac{dv_D}{dT} = \frac{1.942\times 10^{-3}}{0.7} = 2.775\times 10^{-3}$$

Problem 2.5-2
Plot the noise voltage as a function of the frequency if the thermal noise is 100 nV/$\sqrt{\text{Hz}}$ and the junction of the 1/*f* and thermal noise (the 1/*f* noise corner) is 10,000 Hz.



Problem 2.6-1
Given the polysilicon resistor in Fig. P2.6-1 with a resistivity of $\rho = 8\times 10^{-4}$ Ω-cm, calculate the resistance of the structure. Consider only the resistance between contact edges. $\rho_S = 50$ Ω/ ❑

Fix problem: Eliminate . $\rho_S = 50$ Ω/ ❑ because it conflicts with $\rho = 8\times 10^{-4}$ Ω-cm

$$R = \frac{\rho L}{WT} = \frac{8\times10^{-4} \times 3\times10^{-4}}{1\times10^{-4} \times 8000\times10^{-8}} = 30\ \Omega$$

Problem 2.6-2
Given that you wish to match two transistors having a W/L of 100μm/0.8μm each. Sketch the layout of these two transistors to achieve the best possible matching.

Best matching is achieved using the following principles:

- unit matching
- common centroid
- photolithographic invariance

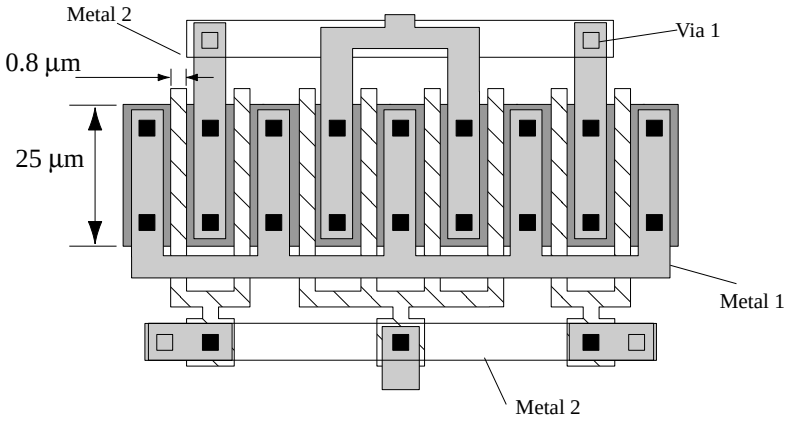


Figure P2.6-2

Problem 2.6-3
Assume that the edge variation of the top plate of a capacitor is 0.05μm and that capacitor top plates are to be laid out as squares. It is desired to match two equal capacitors to an accuracy of 0.1%. Assume that there is no variation in oxide thickness. How large would the capacitors have to be to achieve this matching accuracy?

Since capacitance is dominated by the area component, ignore the perimeter (fringe) component in this analysis. The units in the analysis that follows is micrometers.

$C = C_{\text{AREA}}\ (\text{d} \pm 0.05)^2$

where d is one (both) sides of the square capacitor.

$$\frac{C_1}{C_1} = \frac{(\text{d} + 0.05)^2}{(\text{d} - 0.05)^2} = 1.001$$

$$\frac{C_1}{C_1} = \frac{(d + 0.05)^2}{(d - 0.05)^2} = 1.001$$

$$d^2 + 0.1d + 0.05^2 = 1.001\left(d^2 - 0.1d + 0.05^2\right)$$

Solving this quadratic yields

$$d = 200.1$$

Problem 2.6-4
Show that a circular geometry minimizes perimeter-to-area ratio for a given area requirement. In your proof, compare against rectangle and square.

$$A_{circle} = \pi r^2$$

$$A_{square} = d^2$$

if $A_{square} = A_{circle}$

then

$$r = \frac{d\sqrt{\pi}}{\pi}$$

$$\frac{P_{circle}}{P_{square}} = \frac{2d\sqrt{\pi}}{4d} = \frac{\sqrt{\pi}}{2} < 1$$

Ideally, $\frac{C_{perimeter}}{C_{area}} = 0$, so since $\frac{P_{circle}}{P_{square}} < 1$, the impact of perimeter on a circle is less than on a square.

Problem 2.6-5
Show analytically how the Yiannoulos-path technique illustrated in Fig. 2.6-5 maintains a constant area-to-perimeter ratio with non-integer ratios.

Area of one unit is:

$$A_u = L^2$$

Total area = $N \times A_u$

Total periphery = $2(N + 1)$

$C_{Total} = K_A \times N \times A_u + K_P \times 2(N + 1)$

where K_A and K_P represent area and perimeter capacitance (per unit area and per unit length) respectively.

Consider two capacitors with different numbers of units but drawn following the template shown in Fig. 2.6-5(a). Their ratio would be

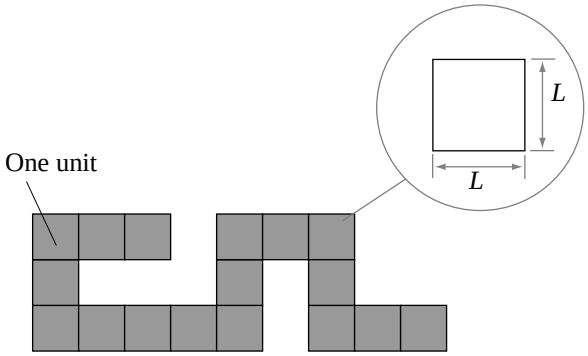


Figure P2.6-5 (a)

$$\frac{C_1}{C_2} = \frac{K_A \times N_1 \times A_u + K_P \times 2(N_1 + 1)}{K_A \times N_2 \times A_u + K_P \times 2(N_2 + 1)}$$

The ratio of the area and peripheral components by themselves are

$$\left(\frac{C_1}{C_2}\right)_{AREA} = \frac{K_A \times N_1 \times A_u}{K_A \times N_2 \times A_u} = \frac{N_1}{N_2}$$

$$\left(\frac{C_1}{C_2}\right)_{PER} = \frac{K_P \times 2(N_1 + 1)}{K_P \times 2(N_2 + 1)} = \frac{N_1 + 1}{N_2 + 1}$$

$$\frac{N_1 + 1}{N_2 + 1} \neq \frac{N_1}{N_2} \text{ unless } N_1 = N_2$$

Therefore, the structure in Fig. P2.6-5(a) cannot achieve constant area to perimeter ratio.

Consider Fig. P2.6-5(b).

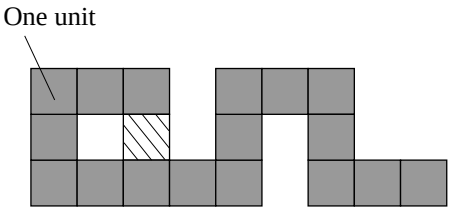


Figure P2.6-5 (b)

Total area = $(N + 1) \times A_u$

Total periphery = $2(N + 1)$ (as before)

Notice what has happened. By adding the extra unit area, two peripheral units are eliminated but two additional ones are added resulting in no change in total periphery. However, one additional area has been added. Thus

$$\frac{C_1}{C_2} = \frac{K_A \times (N_1 + 1) \times A_u + K_P \times 2(N_1 + 1)}{K_A \times (N_2 + 1) \times A_u + K_P \times 2(N_2 + 1)}$$

The ratio of the area and peripheral components by themselves are

$$\left(\frac{C_1}{C_2}\right)_{AREA} = \frac{K_A \times (N_1 + 1) \times A_u}{K_A \times (N_2 + 1) \times A_u} = \frac{N_1 + 1}{N_2 + 1}$$

$$\left(\frac{C_1}{C_2}\right)_{PER} = \frac{K_P \times 2(N_1 + 1)}{K_P \times 2(N_2 + 1)} = \frac{N_1 + 1}{N_2 + 1}$$

$$\frac{N_1 + 1}{N_2 + 1} = \frac{N_1 + 1}{N_2 + 1} \text{ !!!}$$

Problem 2.6-6

Design an optimal layout of a matched pair of transistors whose W/L are 8μm/1μm. The matching should be photolithographic invariant as well as common centroid.

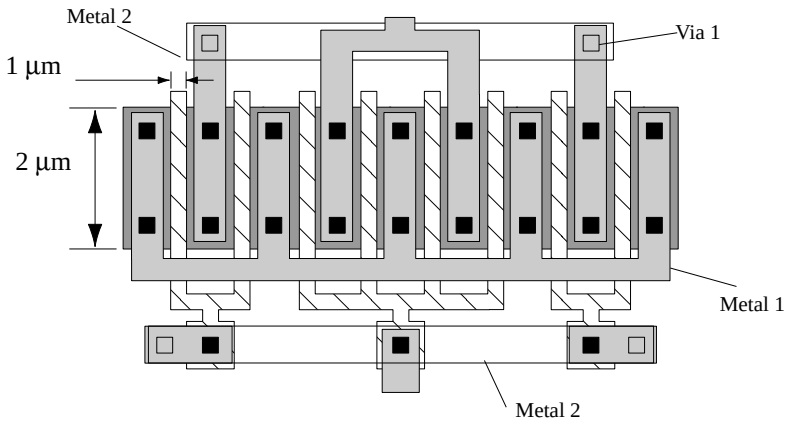


Figure P2.6-6

Problem 2.6-7

Figure P2.6-7 illustrates various ways to implement the layout of a resistor divider. Choose the layout that BEST achieves the goal of a 2:1 ratio. Explain why the other choices are not optimal.

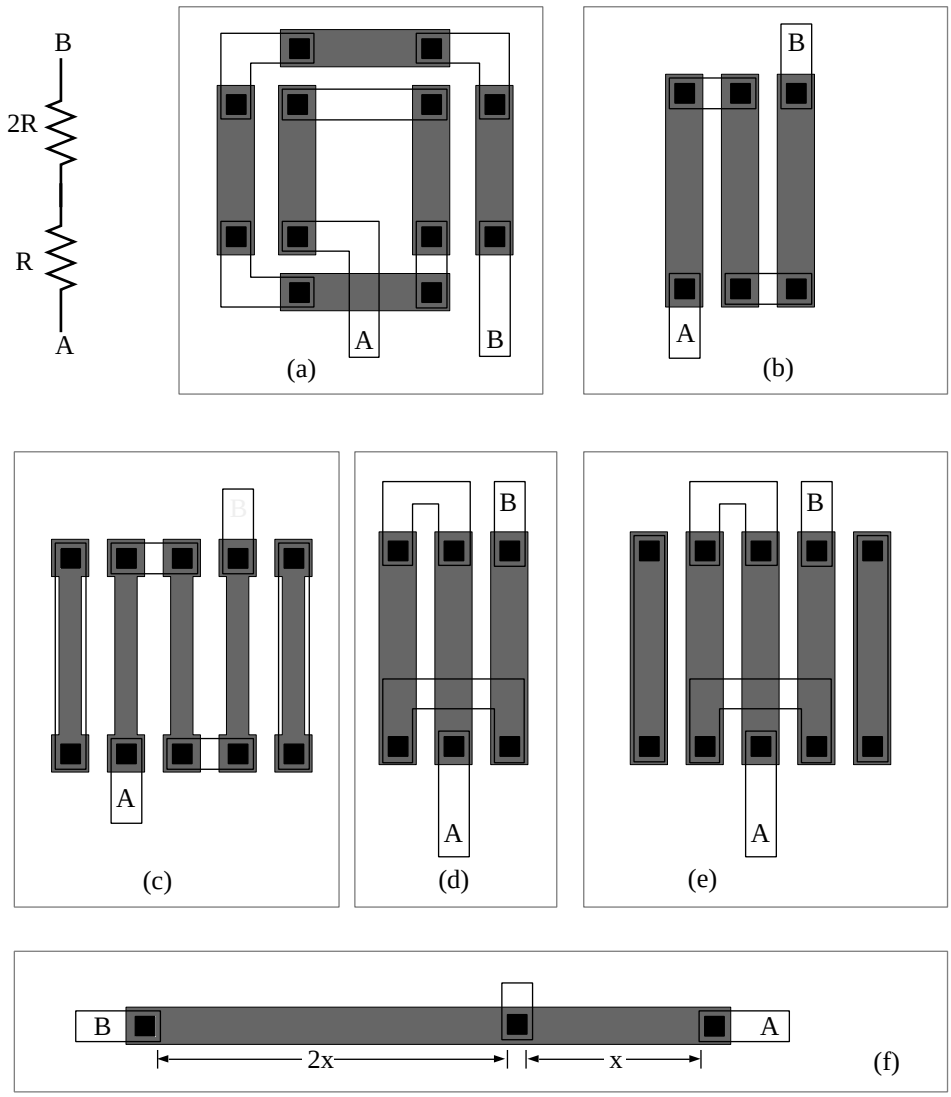


Figure P2.6-7

Option A suffers the following:

- Orientation of the 2R resistor is partly orthogonal to the 1R resistor. Matched resistors should have the same orientation.
- Resistors do not have the appropriate etch compensating (dummy) resistors. Dummy stripes should surround all active resistors.

Option B suffers the following:

- Resistors do not have the appropriate etch compensating (dummy) resistors. Dummy stripes should surround all active resistors.
- Resistors do not share a common centroid as they should.

Option C suffers the following:

- Resistors do not share a common centroid as they should.
- Uncertainty is introduced with the additional notch at the contact head.

Option D suffers the following:

- Resistors do not have the appropriate etch compensating (dummy) resistors. Dummy stripes should surround all active resistors.

Option E suffers the following:

- Nothing

Option F suffers the following:

- Violates the unit-matching principle
- Resistors do not have the appropriate etch compensating (dummy) resistors. Dummy stripes should surround all active resistors.
- Resistors do not share a common centroid as they should.

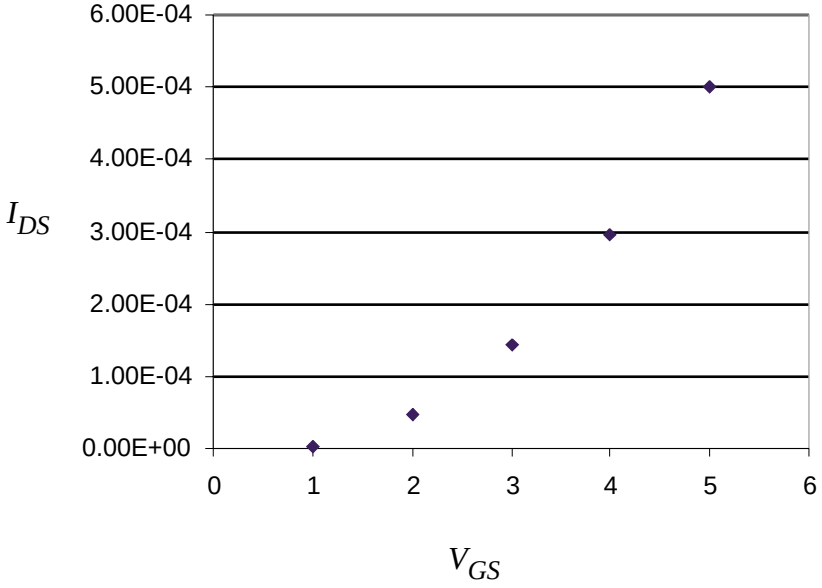
	Unit Matching	Etch Comp.	Orientation	Common Centroid
(a)	Yes	No	No	Yes
(b)	Yes	No	Yes	No
(c)	Yes	Yes	Yes	No
(d)	Yes	No	Yes	Yes
(e)	Yes	Yes	Yes	Yes
(f)	No	No	Yes	No

Clearly, option (e) is the best choice.

Chapter 3 Homework Solutions

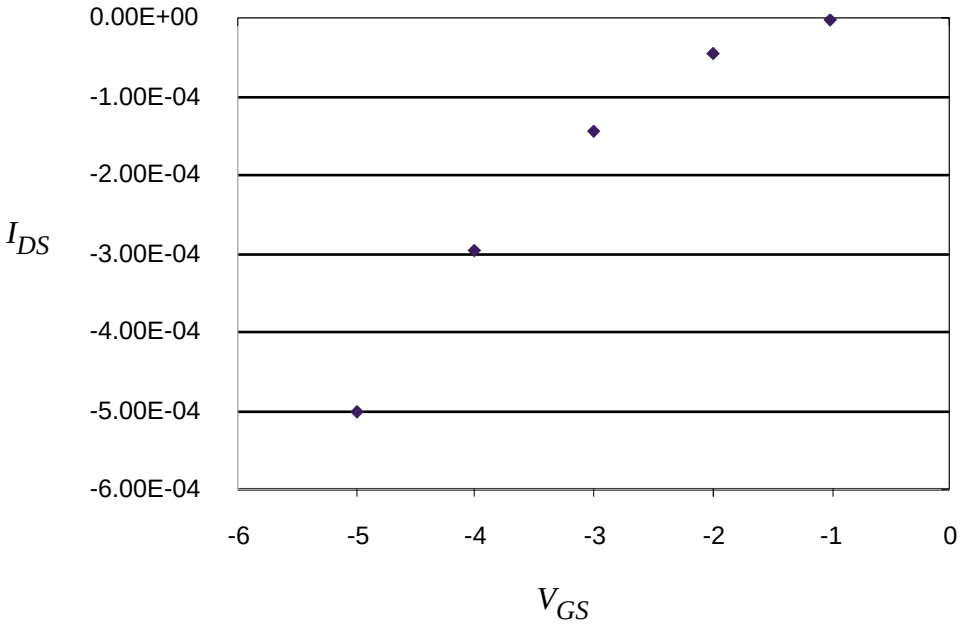
Problem 3.1-1

Sketch to scale the output characteristics of an enhancement n-channel device if $V_T = 0.7$ volt and $I_D = 500$ μA when $V_{GS} = 5$ V in saturation. Choose values of $V_{GS} = 1, 2, 3, 4,$ and 5 V. Assume that the channel modulation parameter is zero.



Problem 3.1-2

Sketch to scale the output characteristics of an enhancement p-channel device if $V_T = -0.7$ volt and $I_D = -500$ μA when $V_{GS} = -1, -2, -3, -4,$ and -6 V. Assume that the channel modulation parameter is zero.



Problem 3.1-3
In Table 3.1-2, why is γ_P greater than γ_N for a n-well, CMOS technology?
The expression for γ is:

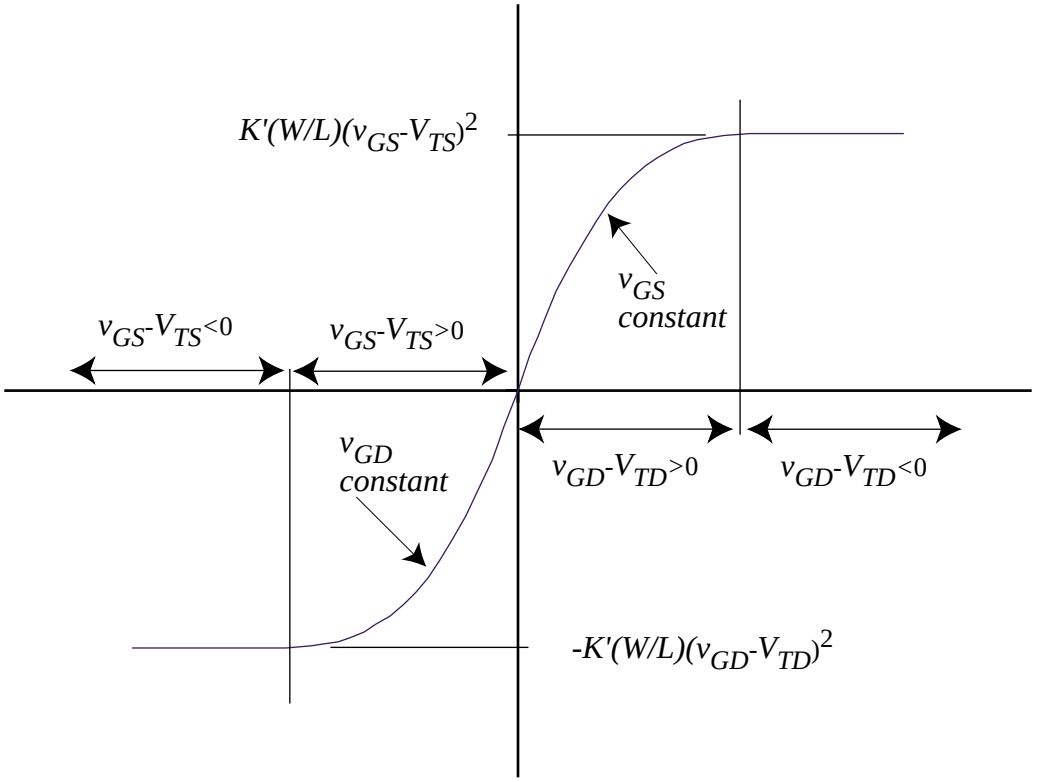
$$\gamma = \frac{\sqrt{2\varepsilon_{si}\, q\, N_{SUB}}}{C_{ox}}$$

Because γ is a function of substrate doping, a higher doping results in a larger value for γ. In general, for an nwell process, the well has a greater doping concentration than the substrate and therefore devices in the well will have a larger γ.

Problem 3.1-4
A large-signal model for the MOSFET which features symmetry for the drain and source is given as

$$i_D = K' \frac{W}{L}\left\{[(v_{GS} - V_{TS})^2\, u(v_{GS} - V_{TS})] - [(v_{GD} - V_{TD})^2\, u(v_{GD} - V_{TD})]\right\}$$

where $u(x)$ is 1 if x is greater than or equal to zero and 0 if x is less than zero (step function) and V_{TX} is the threshold voltage evaluated from the gate to X where X is either S (Source) or D (Drain). Sketch this model in the form of i_D versus v_{DS} for a constant value of v_{GS} ($v_{GS} > V_{TS}$) and identify the saturated and nonsaturated regions. Be sure to extend this sketch for both positive and negative values of v_{DS}. Repeat the sketch of i_D versus v_{DS} for a constant value of v_{GD} ($v_{GD} > V_{TD}$). Assume that both V_{TS} and V_{TD} are positive.



Problem 3.1-5

Equation (3.1-12) and Eq. (3.1-18) describe the MOS model in nonsaturation and saturation region, respectively. These equations do not agree at the point of transition between saturation and nonsaturation regions. For hand calculations, this is not an issue, but for computer analysis, it is. How would you change Eq. (3.1-18) so that it would agree with Eq. (3.1-12) at $v_{DS} = v_{DS}$ (sat)?

$$i_D = K' \frac{W}{L}\left[(v_{GS} - V_T) - \frac{v_{DS}}{2}\right] v_{DS} \qquad (3.1\text{-}12)$$

$$i_D = K' \frac{W}{2L}(v_{GS} - V_T)^2(1 + \lambda v_{DS}), \quad 0 < (v_{GS} - V_T) \le v_{DS} \qquad (3.1\text{-}18)$$

What happens to Eq. 3.1-12 at the point where saturation occurs?

$$i_D = K' \frac{W}{L}\left[(v_{GS} - V_T) - \frac{v_{DS}\,(sat)}{2}\right] v_{DS}(sat)$$

$$v_{DS}\,(sat) = v_{GS} - V_T$$

then

$$i_D = K' \frac{W}{L}\left[(v_{GS} - V_T)\, v_{DS}(sat) - \frac{v_{DS}^2\,(sat)}{2}\right]$$

$$i_D = K' \frac{W}{L}\left[(v_{GS} - V_T)\,(v_{GS} - V_T) - \frac{(v_{GS} - V_T)^2}{2}\right]$$

$$i_D = K' \frac{W}{L}\left[(v_{GS} - V_T)^2 - \frac{(v_{GS} - V_T)^2}{2}\right] = K' \frac{W}{L}\left[\frac{(v_{GS} - V_T)^2}{2}\right]$$

$$i_D = K' \frac{W}{L}\left[\frac{(v_{GS} - V_T)^2}{2}\right]$$

which is not equal to Eq.(3.1-18) because of the channel-length modulation term.

Since Eq. (3.1-18) is valid only during saturation when $v_{DS} > v_{DS}(sat)$ we can subtract $v_{DS}(sat)$ from the v_{DS} in the channel-length modulation term. Doing this results in the following modification of Eq. (3.1-18).

$$i_D = K' \frac{W}{2L}(v_{GS} - V_T)^2\left[1 + \lambda (v_{DS} - v_{DS}(sat))\right], \quad 0 < (v_{GS} - V_T) \le v_{DS}$$

When $v_{DS} = v_{DS}(sat)$, this expression agrees with the non-saturation equation at the point of transition into saturation. Beyond saturation, channel-length modulation is applied to the difference in v_{DS} and $v_{DS}(sat)$.

Problem 3.2-1
Using the values of Tables 3.1-1 and 3.2-1, calculate the values of CGB, CGS, and CGD for a MOS device which has a W of 5 μm and an L of 1 μm for all three regions of operation.

We will need LD in these calculations. LD can be approximated from the value given for CGSO in Table 3.2-1.

$$LD = \frac{220 \times 10^{-12}}{24.7 \times 10^{-4}} \cong 89 \times 10^{-9}$$

Off

$C_{GB} = C_2 + 2C_5 = C_{ox}(W_{\text{eff}})(L_{\text{eff}}) + 2\text{CGBO}(L_{\text{eff}})$

$W_{\text{eff}} = 5\ \mu\text{m}$

$L_{\text{eff}} = 1\ \mu\text{m} - 2\times 89\ \text{nm} = 822 \times 10^{-9}$

$C_{GB} = 24.7 \times 10^{-4} \times (5\times 10^{-6})(822 \times 10^{-9}) + 2\times 700 \times 10^{-12}\times 822 \times 10^{-9}$

$C_{GB} = 11.3 \times 10^{-15}$ F

$C_{GS} = C_1 \cong C_{ox}(\text{LD})(W_{\text{eff}}) = \text{CGSO}(W_{\text{eff}})$

$C_{GS} = (220 \times 10^{-12}) (5 \times 10^{-6}) = 1.1 \times 10^{-15}$

$C_{GD} = C_2 \cong C_{ox}(\text{LD})(W_{\text{eff}}) = \text{CGDO}(W_{\text{eff}})$

$C_{GD} = (220 \times 10^{-12}) (5 \times 10^{-6}) = 1.1 \times 10^{-15}$

Saturation

$C_{GB} = 2C_5 = \text{CGBO}\ (L_{\text{eff}})$