

1

Solutions

1.1 Personal computer (includes workstation and laptop): Personal computers emphasize delivery of good performance to single users at low cost and usually execute third-party software.

Personal mobile device (PMD, includes tablets): PMDs are battery operated with wireless connectivity to the Internet and typically cost hundreds of dollars, and, like PCs, users can download software (“apps”) to run on them. Unlike PCs, they no longer have a keyboard and mouse, and are more likely to rely on a touch-sensitive screen or even speech input.

Server: Computer used to run large problems and usually accessed via a network.

Warehouse scale computer: Thousands of processors forming a large cluster.

Supercomputer: Computer composed of hundreds to thousands of processors and terabytes of memory.

Embedded computer: Computer designed to run one application or one set of related applications and integrated into a single system.

1.2

- a. Performance via Pipelining
- b. Dependability via Redundancy
- c. Performance via Prediction
- d. Make the Common Case Fast
- e. Hierarchy of Memories
- f. Performance via Parallelism
- g. Design for Moore’s Law
- h. Use Abstraction to Simplify Design

1.3 The program is compiled into an assembly language program, which is then assembled into a machine language program.

1.4

- a. $1280 \times 1024 \text{ pixels} = 1,310,720 \text{ pixels} \Rightarrow 1,310,720 \times 3 = 3,932,160 \text{ bytes/frame.}$
- b. $3,932,160 \text{ bytes} \times (8 \text{ bits/byte}) / 100\text{E6 bits/second} = 0.31 \text{ seconds}$

1.5

- a. performance of P1 (instructions/sec) $= 3 \times 10^9 / 1.5 = 2 \times 10^9$
 performance of P2 (instructions/sec) $= 2.5 \times 10^9 / 1.0 = 2.5 \times 10^9$
 performance of P3 (instructions/sec) $= 4 \times 10^9 / 2.2 = 1.8 \times 10^9$

- b. $\text{cycles}(P1) = 10 \times 3 \times 10^9 = 30 \times 10^9 \text{ s}$
 $\text{cycles}(P2) = 10 \times 2.5 \times 10^9 = 25 \times 10^9 \text{ s}$
 $\text{cycles}(P3) = 10 \times 4 \times 10^9 = 40 \times 10^9 \text{ s}$
- c. $\text{No. instructions}(P1) = 30 \times 10^9 / 1.5 = 20 \times 10^9$
 $\text{No. instructions}(P2) = 25 \times 10^9 / 1 = 25 \times 10^9$
 $\text{No. instructions}(P3) = 40 \times 10^9 / 2.2 = 18.18 \times 10^9$
 $\text{CPI}_{\text{new}} = \text{CPI}_{\text{old}} \times 1.2$, then $\text{CPI}(P1) = 1.8$, $\text{CPI}(P2) = 1.2$, $\text{CPI}(P3) = 2.6$
 $f = \text{No. instr.} \times \text{CPI} / \text{time}$, then
 $f(P1) = 20 \times 10^9 \times 1.8 / 7 = 5.14 \text{ GHz}$
 $f(P2) = 25 \times 10^9 \times 1.2 / 7 = 4.28 \text{ GHz}$
 $f(P3) = 18.18 \times 10^9 \times 2.6 / 7 = 6.75 \text{ GHz}$

1.6

- a. Class A: 10^5 instr. Class B: 2×10^5 instr. Class C: 5×10^5 instr.
Class D: 2×10^5 instr.
 $\text{Time} = \text{No. instr.} \times \text{CPI} / \text{clock rate}$
 $\text{Total time P1} = (10^5 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3) / (2.5 \times 10^9) = 10.4 \times 10^{-4} \text{ s}$
 $\text{Total time P2} = (10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2) / (3 \times 10^9) = 6.66 \times 10^{-4} \text{ s}$
 $\text{CPI}(P1) = 10.4 \times 10^{-4} \times 2.5 \times 10^9 / 10^6 = 2.6$
 $\text{CPI}(P2) = 6.66 \times 10^{-4} \times 3 \times 10^9 / 10^6 = 2.0$
- b. $\text{clock cycles}(P1) = 10^5 \times 1 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3 = 26 \times 10^5$
 $\text{clock cycles}(P2) = 10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2 = 20 \times 10^5$

1.7

- a. $\text{CPI} = T_{\text{exec}} \times f / \text{No. instr.}$
Compiler A $\text{CPI} = 1.1$
Compiler B $\text{CPI} = 1.25$
- b. $f_B / f_A = (\text{No. instr.}(B) \times \text{CPI}(B)) / (\text{No. instr.}(A) \times \text{CPI}(A)) = 1.37$
- c. $T_A / T_{\text{new}} = 1.67$
 $T_B / T_{\text{new}} = 2.27$

1.8

$$1.8.1 \quad C = 2 \times DP/(V^2 \times F)$$

$$\text{Pentium 4: } C = 3.2\text{E-}8F$$

$$\text{Core i5 Ivy Bridge: } C = 2.9\text{E-}8F$$

$$1.8.2 \quad \text{Pentium 4: } 10/100 = 10\%$$

$$\text{Core i5 Ivy Bridge: } 30/70 = 42.9\%$$

$$1.8.3 \quad (S_{\text{new}} + D_{\text{new}})/(S_{\text{old}} + D_{\text{old}}) = 0.90$$

$$D_{\text{new}} = C \times V_{\text{new}}^2 \times F$$

$$S_{\text{old}} = V_{\text{old}} \times I$$

$$S_{\text{new}} = V_{\text{new}} \times I$$

Therefore:

$$V_{\text{new}} = [D_{\text{new}}/(C \times F)]^{1/2}$$

$$D_{\text{new}} = 0.90 \times (S_{\text{old}} + D_{\text{old}}) - S_{\text{new}}$$

$$S_{\text{new}} = V_{\text{new}} \times (S_{\text{old}}/V_{\text{old}})$$

Pentium 4:

$$S_{\text{new}} = V_{\text{new}} \times (10/1.25) = V_{\text{new}} \times 8$$

$$D_{\text{new}} = 0.90 \times 100 - V_{\text{new}} \times 8 = 90 - V_{\text{new}} \times 8$$

$$V_{\text{new}} = [(90 - V_{\text{new}} \times 8)/(3.2\text{E}8 \times 3.6\text{E}9)]^{1/2}$$

$$V_{\text{new}} = 0.85 \text{ V}$$

Core i5:

$$S_{\text{new}} = V_{\text{new}} \times (30/0.9) = V_{\text{new}} \times 33.3$$

$$D_{\text{new}} = 0.90 \times 70 - V_{\text{new}} \times 33.3 = 63 - V_{\text{new}} \times 33.3$$

$$V_{\text{new}} = [(63 - V_{\text{new}} \times 33.3)/(2.9\text{E}8 \times 3.4\text{E}9)]^{1/2}$$

$$V_{\text{new}} = 0.64 \text{ V}$$

1.9**1.9.1**

p	# arith inst.	# L/S inst.	# branch inst.	cycles	ex. time	speedup
1	2.56E9	1.28E9	2.56E8	7.94E10	39.7	1
2	1.83E9	9.14E8	2.56E8	5.67E10	28.3	1.4
4	9.12E8	4.57E8	2.56E8	2.83E10	14.2	2.8
8	4.57E8	2.29E8	2.56E8	1.42E10	7.10	5.6

1.9.2

p	ex. time
1	41.0
2	29.3
4	14.6
8	7.33

1.9.3 3

1.10

$$1.10.1 \text{ die area}_{15\text{cm}} = \text{wafer area/dies per wafer} = \pi \cdot 7.5^2 / 84 = 2.10 \text{ cm}^2$$

$$\text{yield}_{15\text{cm}} = 1/(1 + (0.020 \cdot 2.10/2))^2 = 0.9593$$

$$\text{die area}_{20\text{cm}} = \text{wafer area/dies per wafer} = \pi \cdot 10^2 / 100 = 3.14 \text{ cm}^2$$

$$\text{yield}_{20\text{cm}} = 1/(1 + (0.031 \cdot 3.14/2))^2 = 0.9093$$

$$1.10.2 \text{ cost/die}_{15\text{cm}} = 12/(84 \cdot 0.9593) = 0.1489$$

$$\text{cost/die}_{20\text{cm}} = 15/(100 \cdot 0.9093) = 0.1650$$

$$1.10.3 \text{ die area}_{15\text{cm}} = \text{wafer area/dies per wafer} = \pi \cdot 7.5^2 / (84 \cdot 1.1) = 1.91 \text{ cm}^2$$

$$\text{yield}_{15\text{cm}} = 1/(1 + (0.020 \cdot 1.15 \cdot 1.91/2))^2 = 0.9575$$

$$\text{die area}_{20\text{cm}} = \text{wafer area/dies per wafer} = \pi \cdot 10^2 / (100 \cdot 1.1) = 2.86 \text{ cm}^2$$

$$\text{yield}_{20\text{cm}} = 1/(1 + (0.03 \cdot 1.15 \cdot 2.86/2))^2 = 0.9082$$

$$1.10.4 \text{ defects per area}_{0.92} = (1 - y^{.5}) / (y^{.5} \cdot \text{die_area}/2) = (1 - 0.92^{.5}) / (0.92^{.5} \cdot 2/2) = 0.043 \text{ defects/cm}^2$$

$$\text{defects per area}_{0.95} = (1 - y^{.5}) / (y^{.5} \cdot \text{die_area}/2) = (1 - 0.95^{.5}) / (0.95^{.5} \cdot 2/2) = 0.026 \text{ defects/cm}^2$$

1.11

$$1.11.1 \text{ CPI} = \text{clock rate} \times \text{CPU time/instr. count}$$

$$\text{clock rate} = 1/\text{cycle time} = 3 \text{ GHz}$$

$$\text{CPI}(\text{bzip2}) = 3 \times 10^9 \times 750 / (2389 \times 10^9) = 0.94$$

$$1.11.2 \text{ SPEC ratio} = \text{ref. time/execution time}$$

$$\text{SPEC ratio}(\text{bzip2}) = 9650/750 = 12.86$$

$$1.11.3. \text{ CPU time} = \text{No. instr.} \times \text{CPI/clock rate}$$

If CPI and clock rate do not change, the CPU time increase is equal to the increase in the of number of instructions, that is 10%.

$$1.11.4 \text{ CPU time(before)} = \text{No. instr.} \times \text{CPI/clock rate}$$

$$\text{CPU time(after)} = 1.1 \times \text{No. instr.} \times 1.05 \times \text{CPI/clock rate}$$

$\text{CPU time(after)}/\text{CPU time(before)} = 1.1 \times 1.05 = 1.155$. Thus, CPU time is increased by 15.5%.

$$1.11.5 \text{ SPECratio} = \text{reference time}/\text{CPU time}$$

$$\text{SPECratio(after)}/\text{SPECratio(before)} = \text{CPU time(before)}/\text{CPU time(after)} = 1/1.155 = 0.86. \text{ The SPECratio is decreased by 14\%.}$$

$$1.11.6 \text{ CPI} = (\text{CPU time} \times \text{clock rate})/\text{No. instr.}$$

$$\text{CPI} = 700 \times 4 \times 10^9 / (0.85 \times 2389 \times 10^9) = 1.37$$

$$1.11.7 \text{ Clock rate ratio} = 4 \text{ GHz}/3 \text{ GHz} = 1.33$$

$$\text{CPI @ 4 GHz} = 1.37, \text{ CPI @ 3 GHz} = 0.94, \text{ ratio} = 1.45$$

They are different because, although the number of instructions has been reduced by 15%, the CPU time has been reduced by a lower percentage.

$$1.11.8 \text{ } 700/750 = 0.933. \text{ CPU time reduction: 6.7\%}$$

$$1.11.9 \text{ No. instr.} = \text{CPU time} \times \text{clock rate}/\text{CPI}$$

$$\text{No. instr.} = 960 \times 0.9 \times 4 \times 10^9 / 1.61 = 2146 \times 10^9$$

$$1.11.10 \text{ Clock rate} = \text{No. instr.} \times \text{CPI}/\text{CPU time.}$$

$$\text{Clock rate}_{\text{new}} = \text{No. instr.} \times \text{CPI}/0.9 \times \text{CPU time} = 1/0.9 \text{ clock rate}_{\text{old}} = 3.33 \text{ GHz}$$

$$1.11.11 \text{ Clock rate} = \text{No. instr.} \times \text{CPI}/\text{CPU time.}$$

$$\text{Clock rate}_{\text{new}} = \text{No. instr.} \times 0.85 \times \text{CPI}/0.80 \text{ CPU time} = 0.85/0.80, \text{ clock rate}_{\text{old}} = 3.18 \text{ GHz}$$

1.12

$$1.12.1 \text{ } T(P1) = 5 \times 10^9 \times 0.9 / (4 \times 10^9) = 1.125 \text{ s}$$

$$T(P2) = 10^9 \times 0.75 / (3 \times 10^9) = 0.25 \text{ s}$$

$\text{clock rate (P1)} > \text{clock rate(P2)}, \text{ performance(P1)} < \text{performance(P2)}$

$$1.12.2 \text{ } T(P1) = \text{No. instr.} \times \text{CPI}/\text{clock rate}$$

$$T(P1) = 2.25 \times 10^{21} \text{ s}$$

$$T(P2) \text{ } 5 \times 10^9 \times 0.75 / (3 \times 10^9), \text{ then } N = 9 \times 10^8$$

$$1.12.3 \text{ MIPS} = \text{Clock rate} \times 10^{-6}/\text{CPI}$$

$$\text{MIPS(P1)} = 4 \times 10^9 \times 10^{-6}/0.9 = 4.44 \times 10^3$$

$$\text{MIPS(P2)} = 3 \times 10^9 \times 10^{-6} / 0.75 = 4.0 \times 10^3$$

$\text{MIPS(P1)} > \text{MIPS(P2)}$, $\text{performance(P1)} < \text{performance(P2)}$ (from 11a)

$$\mathbf{1.12.4} \quad \text{MFLOPS} = \text{No. FP operations} \times 10^{-6} / T$$

$$\text{MFLOPS(P1)} = .4 \times 5\text{E}9 \times 1\text{E}-6 / 1.125 = 1.78\text{E}3$$

$$\text{MFLOPS(P2)} = .4 \times 1\text{E}9 \times 1\text{E}-6 / .25 = 1.60\text{E}3$$

$\text{MFLOPS(P1)} > \text{MFLOPS(P2)}$, $\text{performance(P1)} < \text{performance(P2)}$ (from 11a)

1.13

$$\mathbf{1.13.1} \quad T_{\text{fp}} = 70 \times 0.8 = 56 \text{ s. } T_{\text{new}} = 56 + 85 + 55 + 40 = 236 \text{ s. Reduction: 5.6\%}$$

$$\mathbf{1.13.2} \quad T_{\text{new}} = 250 \times 0.8 = 200 \text{ s, } T_{\text{fp}} + T_{\text{l/s}} + T_{\text{branch}} = 165 \text{ s, } T_{\text{int}} = 35 \text{ s. Reduction time INT: 58.8\%}$$

$$\mathbf{1.13.3} \quad T_{\text{new}} = 250 \times 0.8 = 200 \text{ s, } T_{\text{fp}} + T_{\text{int}} + T_{\text{l/s}} = 210 \text{ s. NO}$$

1.14

$$\mathbf{1.14.1} \quad \text{Clock cycles} = \text{CPI}_{\text{fp}} \times \text{No. FP instr.} + \text{CPI}_{\text{int}} \times \text{No. INT instr.} + \text{CPI}_{\text{l/s}} \times \text{No. L/S instr.} + \text{CPI}_{\text{branch}} \times \text{No. branch instr.}$$

$$T_{\text{CPU}} = \text{clock cycles} / \text{clock rate} = \text{clock cycles} / 2 \times 10^9$$

$$\text{clock cycles} = 512 \times 10^6; T_{\text{CPU}} = 0.256 \text{ s}$$

To have the number of clock cycles by improving the CPI of FP instructions:

$$\text{CPI}_{\text{improved fp}} \times \text{No. FP instr.} + \text{CPI}_{\text{int}} \times \text{No. INT instr.} + \text{CPI}_{\text{l/s}} \times \text{No. L/S instr.} + \text{CPI}_{\text{branch}} \times \text{No. branch instr.} = \text{clock cycles} / 2$$

$$\text{CPI}_{\text{improved fp}} = (\text{clock cycles} / 2 - (\text{CPI}_{\text{int}} \times \text{No. INT instr.} + \text{CPI}_{\text{l/s}} \times \text{No. L/S instr.} + \text{CPI}_{\text{branch}} \times \text{No. branch instr.})) / \text{No. FP instr.}$$

$$\text{CPI}_{\text{improved fp}} = (256 - 462) / 50 < 0 ==> \text{not possible}$$

$$\mathbf{1.14.2} \quad \text{Using the clock cycle data from a.}$$

To have the number of clock cycles improving the CPI of L/S instructions:

$$\text{CPI}_{\text{fp}} \times \text{No. FP instr.} + \text{CPI}_{\text{int}} \times \text{No. INT instr.} + \text{CPI}_{\text{improved l/s}} \times \text{No. L/S instr.} + \text{CPI}_{\text{branch}} \times \text{No. branch instr.} = \text{clock cycles} / 2$$

$$\text{CPI}_{\text{improved l/s}} = (\text{clock cycles} / 2 - (\text{CPI}_{\text{fp}} \times \text{No. FP instr.} + \text{CPI}_{\text{int}} \times \text{No. INT instr.} + \text{CPI}_{\text{branch}} \times \text{No. branch instr.})) / \text{No. L/S instr.}$$

$$\text{CPI}_{\text{improved l/s}} = (256 - 198) / 80 = 0.725$$

$$\mathbf{1.14.3} \quad \text{Clock cycles} = \text{CPI}_{\text{fp}} \times \text{No. FP instr.} + \text{CPI}_{\text{int}} \times \text{No. INT instr.} + \text{CPI}_{\text{l/s}} \times \text{No. L/S instr.} + \text{CPI}_{\text{branch}} \times \text{No. branch instr.}$$

$T_{\text{CPU}} = \text{clock cycles}/\text{clock rate} = \text{clock cycles}/2 \times 10^9$

$\text{CPI}_{\text{int}} = 0.6 \times 1 = 0.6$; $\text{CPI}_{\text{fp}} = 0.6 \times 1 = 0.6$; $\text{CPI}_{\text{l/s}} = 0.7 \times 4 = 2.8$;
 $\text{CPI}_{\text{branch}} = 0.7 \times 2 = 1.4$

$T_{\text{CPU}} (\text{before improv.}) = 0.256 \text{ s}$; $T_{\text{CPU}} (\text{after improv.}) = 0.171 \text{ s}$

1.15

processors	exec. time/ processor	time w/overhead	speedup	actual speedup/ideal speedup
1	100			
2	50	54	$100/54 = 1.85$	$1.85/2 = .93$
4	25	29	$100/29 = 3.44$	$3.44/4 = 0.86$
8	12.5	16.5	$100/16.5 = 6.06$	$6.06/8 = 0.75$
16	6.25	10.25	$100/10.25 = 9.76$	$9.76/16 = 0.61$