Instructor's Resource Manual
to accompany

DIGITAL ELECTRONICS
A Practical Approach

Eighth Edition

William Kleitz

Containing

Solutions and Answers to In-Text Problems
William Kleitz, Tompkins Cortland Community College

Solutions to Standard Logic Laboratory Manual
Michael Wiesner and Vance Venable

Test Item File
Sohail Anwar

Upper Saddle River, New Jersey
Columbus, Ohio

10 9 8 7 6 5 4 3 2 1
ISBN-13: 978-0-13-175736-3
ISBN-10: 0-13-175736-9

10 9 8 7 6 5 4 3 2 1
ISBN-13: 978-0-13-243579-6
ISBN-10: 0-13-243579-9

Preface

This *Instructor's Resource Manual* is part of the extensive package of ancillary material available to enhance the teaching and learning process. These products represent the most thorough selection of print, electronic, multimedia, and Internet tools available. This package underscores Prentice Hall's commitment to enable you to prepare and deliver readily the best content presentations and student learning and testing tools. These products very effectively complement the parent textbook, *Digital Electronics: A Practical Approach, Eighth Edition,* the best-selling work in this discipline by respected author William Kleitz.

Components in this *Instructor's Resource Manual* are:

- Solutions and Answers to In-text Problems, by William Kleitz
- Solutions to the Standard Logic *Laboratory Manual to accompany Digital Electronics* (ISBN 0-13-223982-5), by Michael Wiesner and Vance Venable.
- Test Item File containing over 1000 additional multiple-choice questions that can be used to develop weekly quizzes, tests, or final exams.

Other parts of the overall ancillary package from Prentice Hall are:

- Two CD-ROM's packaged with each copy of the parent textbook, containing:
  Selected schematics from the text rendered in Multisim 6.0, 7.0, 8.0, and 9.0.
  Solutions to in-text Altera CPLD examples
  Solutions to in-text Xilinx CPLD examples
  Texas Instruments' fixed-function data sheets
- PowerPoint slides on CD-ROM (ISBN 0-13-223981-7) containing:
  All figures from the text
  Lecture notes for all chapters
  Also available online.
- Three Laboratory Manuals
  1. Standard Logic
     Laboratory Manual to accompany Digital Electronics, by Michael Wiesner and Vance Venable (ISBN 0-13-223982-5)
  2. Altera CPLDs
     Digital Logic Simulation and CPLD Programming, by Steve Waterman (DeVry University) (ISBN 0-13-171514-3)
  3. Xilinx CPLDs
     Digital Electronics Laboratory Experiments, by James Stewart and Chao-Ying Wang (DeVry University) (ISBN 0-13-113124-9)
- *TestGen*, a computerized test bank for producing customized tests and quizzes (ISBN 0-13-243607-8)
- *Companion Website*, a student resource containing additional multiple-choice questions and other textbook-related links, found at http://www.prenhall.com/kleitz

For more information about these supplements, contact your Prentice Hall sales representative. And for more information about other new technology products, visit www.prenhall.com

Contents

Solutions and Answers to In-text Problems

Chapter 1

1–1. **(a)** 6_{10} **(b)** 11_{10} **(c)** 9_{10} **(d)** 7_{10} **(e)** 12_{10} **(f)** 75_{10} **(g)** 55_{10} **(h)** 181_{10} **(i)** 167_{10} **(j)** 118_{10}

1–2. **(a)** $1011\ 1010_2$ **(b)** $1101\ 0110_2$ **(c)** $0001\ 1011_2$ **(d)** $1111\ 1011_2$ **(e)** $1001\ 0010_2$

1–3. **(a)** 31_8 **(b)** 35_8 **(c)** 134_8 **(d)** 131_8 **(e)** 155_8

1–4. **(a)** $100\ 110_2$ **(b)** $111\ 100_2$ **(c)** $110\ 001_2$ **(d)** $011\ 010_2$ **(e)** $101\ 111_2$

1–5. **(a)** 23_{10} **(b)** 31_{10} **(c)** 12_{10} **(d)** 58_{10} **(e)** 41_{10}

1–6. **(a)** 176_8 **(b)** 61_8 **(c)** 127_8 **(d)** 136_8 **(e)** 154_8

1–7. **(a)** $B9_{16}$ **(b)** DC_{16} **(c)** 74_{16} **(d)** FB_{16} **(e)** $C6_{16}$

1–8. **(a)** $1100\ 0101_2$ **(b)** $1111\ 1010_2$ **(c)** $1101\ 0110_2$ **(d)** $1010\ 1001\ 0100_2$ **(e)** $0110\ 0010_2$

1–9. **(a)** 134_{10} **(b)** 244_{10} **(c)** 146_{10} **(d)** 171_{10} **(e)** 965_{10}

1–10. **(a)** $7F_{16}$ **(b)** 44_{16} **(c)** $6B_{16}$ **(d)** $3D_{16}$ **(e)** $1D_{16}$

1–11. **(a)** 98_{10} **(b)** 69_{10} **(c)** 74_{10} **(d)** 36_{10} **(e)** 81_{10}

1–12. **(a)** $1000\ 0111_{BCD}$ **(b)** $0001\ 0100\ 0010_{BCD}$ **(c)** $1001\ 0100_{BCD}$ **(d)** $0110\ 0001_{BCD}$ **(e)** $0100\ 0100_{BCD}$

1–13. **(a)** 010 0101
(b) 0100100 0110001 0110100
(c) 1001110 0101101 0110110
(d) 1000011 1010000 1010101
(e) 1010000 1100111

1–14. **(a)** 25 **(b)** 243134 **(c)** 4E2D36 **(d)** 435055 **(e)** 5067

1–15. **(a)** Tank A, temperature high; tank C, pressure high
(b) Tank D, temperature and pressure high
(c) Tanks B and D, pressure high
(d) Tanks B and C, temperature high
(e) Tank C, temperature and pressure high

1–16. $0001\ 0010\ 0000_{BCD}$

1–17. **(a)** sku43 **(b)** $534B553433_{16}$

1–18. **(a)** 68HC11EMFN, C3 **(b)** 27C64, A8 **(c)** 2N3904, F4 **(d)** DB9, E1

1–19. 16-MAR 1995 Revision A

1–20. **(a)** 2 **(b)** 2 **(c)** 4 **(d)** 1

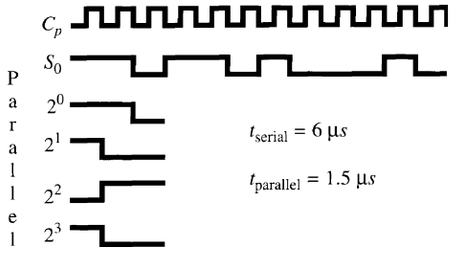
E1–1. **(a)** 0000 0101
(b) Eleven
(c) 0E
(d) 27

E1–2. **(a)** 40
(b) 55
(c) Tank B pressure and temperature are HIGH.
(d) All pressures are HIGH.

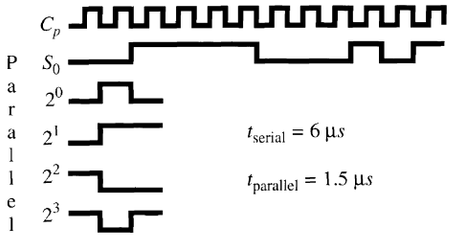
Chapter 2

2–1. **(a)** $t_p = 1/2\text{ MHz} = 0.5\ \mu\text{s}$
(b) $t_p = 1/500\text{ kHz} = 2\ \mu\text{s}$
(c) $t_p = 1/4.27\text{ MHz} = 0.234\ \mu\text{s}$
(d) $t_p = 1/17\text{ MHz} = 58.8\text{ ns}$
(e) $f = 1/2\ \mu\text{s} = 500\text{ kHz}$
(f) $f = 1/100\ \mu\text{s} = 10\text{ kHz}$
(g) $f = 1/0.75\text{ ms} = 1.33\text{ kHz}$
(h) $f = 1/1.5\ \mu\text{s} = 0.667\text{ MHz}$

2–2. **(a)**



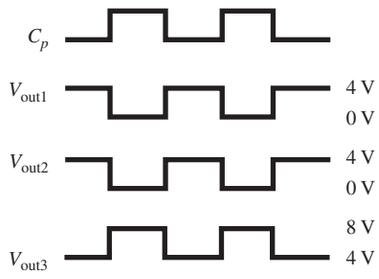
(b)



2–3. **(a)** $8 \times (1/3.7\text{ MHz}) = 2.16\ \mu\text{s}$
(b) 1.21 μs occurs during the 5th period which is LOW.

2–4. **(a)** $3 \times (1/8\text{ MHz}) = 0.375\ \mu\text{s}$
(b) $6 \times (1/4.17\text{ MHz}) = 1.44\ \mu\text{s}$

2–5.



2–6. D_1 = REV D_8 = REV
D_2 = FOR D_9 = REV
D_3 = FOR D_{10} = REV
D_4 = REV D_{11} = REV
D_5 = REV D_{12} = REV
D_6 = REV D_{13} = REV
D_7 = FOR

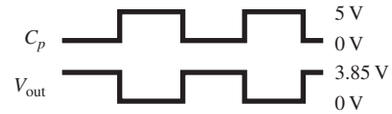
2–7. $V_1 = 0\text{ V}$ $V_5 = 4.3\text{ V}$
$V_2 = 4.3\text{ V}$ $V_6 = 5.0\text{ V}$
$V_3 = 4.3\text{ V}$ $V_7 = 0\text{ V}$
$V_4 = 0\text{ V}$

2–8. That diode will conduct, lowering V_6 to 0.7 V ("AND").

2–9. That diode will conduct, raising V_7 to 4.3 V ("OR").

2–10. $V_{out1} \approx 0\text{ V}$, $V_{out2} \approx 5\text{ V}$

2–11.



2–12. Input signal to BASE (B); output signal from COLLECTOR (C).

2–13. The transistor is cutoff;
$V_{out} = 5\text{ V} \times 1\text{M}\ \Omega/(330\ \Omega + 1\ \text{M}\Omega)$
$V_{out} = 4.998\text{ V}$

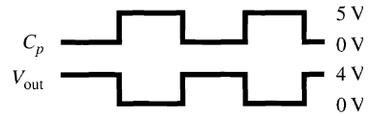
2–14. V_{out} is lowered with a smaller load resistor;
$V_{out} = 5\text{ V} \times 470\ \Omega/(330\ \Omega + 470\ \Omega)$
$V_{out} = 2.94\text{ V}$

2–15. Because, when the transistor is turned on (saturated), the collector current will be excessive ($I_C = 5\text{ V}/R_C$).

2–16. $I_C = 5\text{ V}/100\ \Omega = 50\text{ mA}$

2–17. The totem-pole output replaces R_C with a transistor that acts like a variable resistor. The transistor prevents excessive collector current when it is cut off and provides a high-level output when turned on.

2–18.



2–19. **(a)** 8.0 MHz **(b)** 125 ns

2–20. **(a)** 9.8304 MHz **(b)** 101.73 ns

2–21. P3 parallel, P2 serial

2–22. reverse

2–23. A HIGH on pin 2 will turn Q1 on, making RESET_B approximately zero.

E2–1. **(a)** Let
(b) 24

E2–2. **(a)** Sit
(b) 3

E2–3. **(a)** Cp = 5V/0V, Vout3 = 0V/5V inverse of each other
(b) Cp = 5V/0V, Vout3 = 0V/8V
(c) Cp and Vout3 are in phase.

E2–4. **(a)** Cp = 5V/0V, Vout3 = 10V/6V, in phase
(b) Cp = 5V/0V, Vout3 = 10V/8V
(c) it would be inverted.

E2–5. **(a)** V1 = 4.3V, V2 = 0V, V3 = 4.3V, V4 = 0.7V
(b) V1 = 0V, V2 = 4.3V, V3 = 0V, V4 = 5.0V (Both diodes are reverse biased.)

E2–6. **(a)** Cp = 5V/0V, Vout = 0V/5V, inverse of each other
(b) Cp = 5V/0V, Vout = 0V/8V

Chapter 3

3–1. **(a)**

A	*B*	*C*	*X*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

(b)

A	*B*	*C*	*D*	*X*
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

3–2. $2^8 = 256$

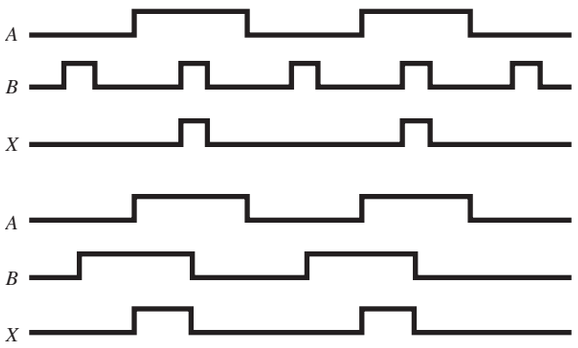
3–3. **(a)** The output is HIGH whenever all inputs are HIGH; otherwise, the output is LOW.
(b) The output is HIGH whenever any input is HIGH; otherwise, the output is LOW.

3–4. $W = 0, X = 1, Y = 0, Z = 0$

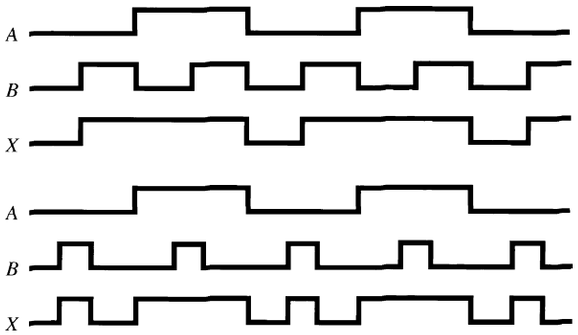
3–5. $X = ABC$
$X = ABCD$
$X = A + B + C$

3–6. $W = 1, X = 0, Y = 1, Z = 1$

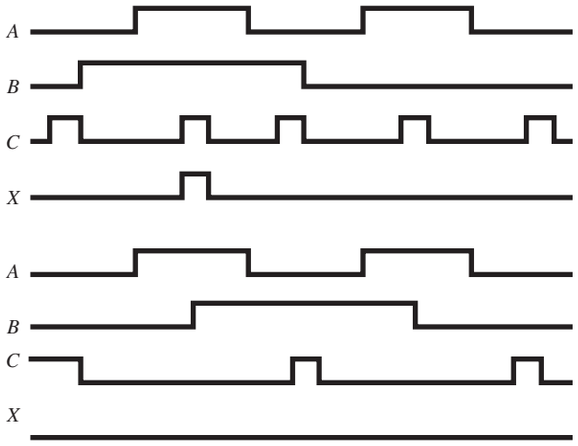
3–7.



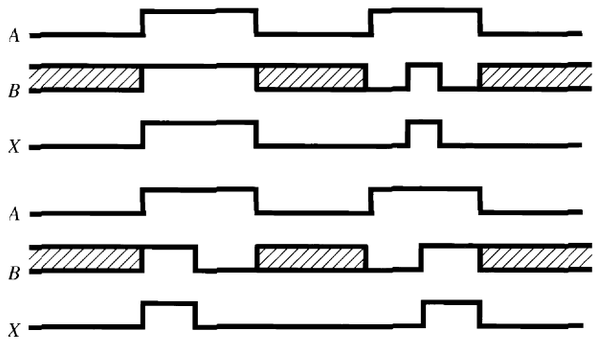
3–8.



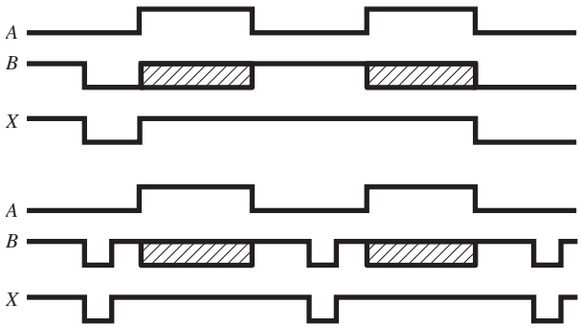
3–9.



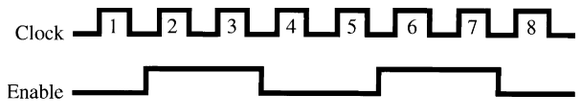
3–10.



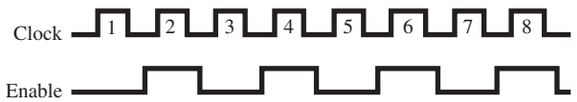
3–11.



3–12.

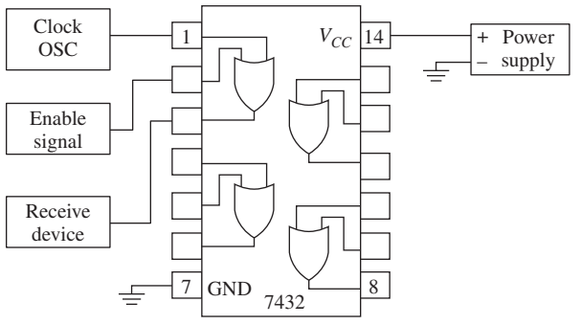


3–13.



3–14. Four

3–15.



3–16. Four

3–17. Two

3–18. HIGH, LOW, and FLOAT

3–19. To provide pulses to a digital circuit for troubleshooting purposes.

3–20. LOW, to enable the output to change with pulser (if gate is good).

3–21. HIGH, to enable the output to change with pulser (if gate is good).

3–22. Pin 3 should be flashing; the AND gate is bad.

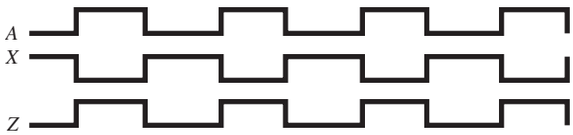
3–23. Pin 2 should be ON; the Enable switch is bad, or bad Enable connection.

3–24. Pin 3 should be flashing and pin 7 should be OFF. There is a bad ground connection to pin 7.

3–25. $X = \overline{A}, X = 0$

3–26. $X = \overline{A}, Z = A, X = 1, Z = 0$

3–27.



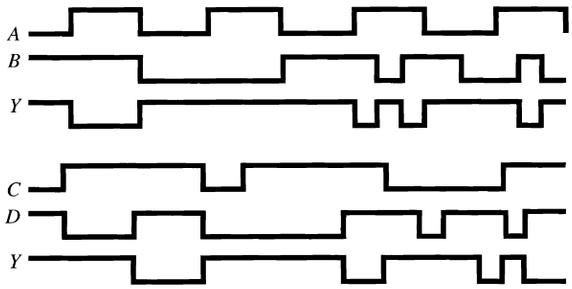
3–28. $X = \overline{AB}$, $Y = \overline{CD}$

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

C	D	Y
0	0	1
0	1	1
1	0	1
1	1	0

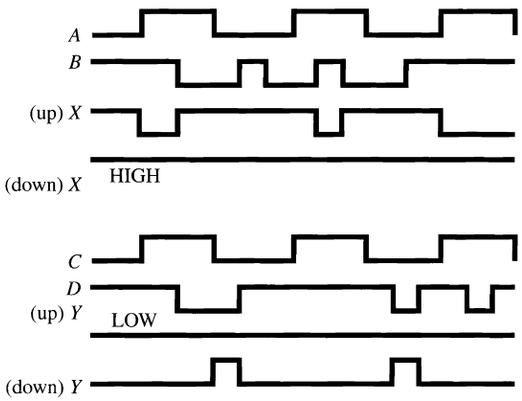
3–29. $W = 1$
$X = 1$
$Y = 1$
$Z = 0$

3–30.



3–31. $W = 1$
$X = 0$
$Y = 0$
$Z = 0$

3–32.



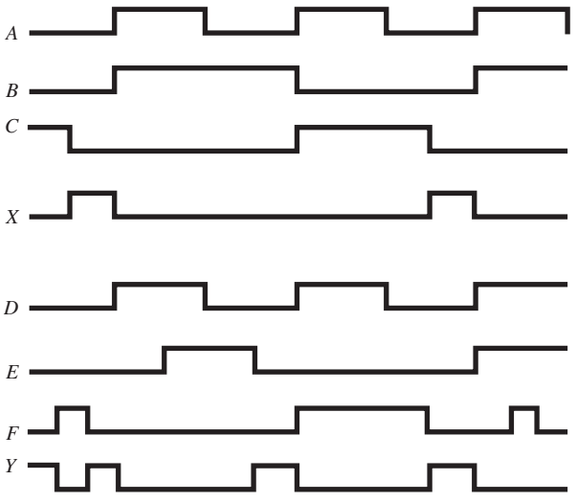
3–33. It disables the other two inputs when it is DOWN for the NAND and UP for the NOR.

3–34. $X = \overline{A + B + C}$ $Y = \overline{D + E + F}$

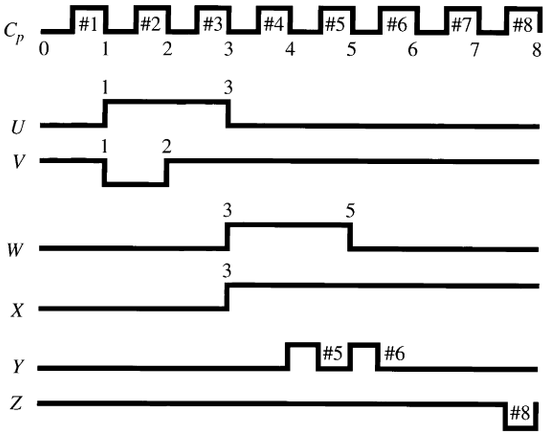
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

D	E	F	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

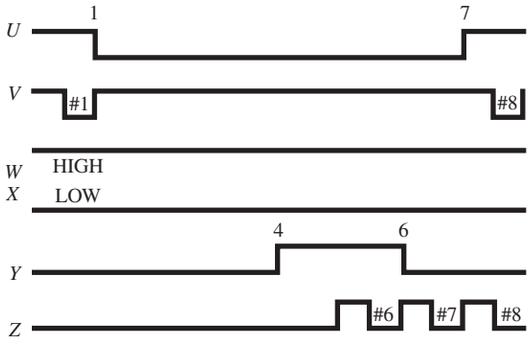
3–35.



3–36.



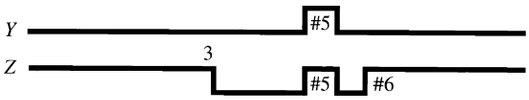
3–37.



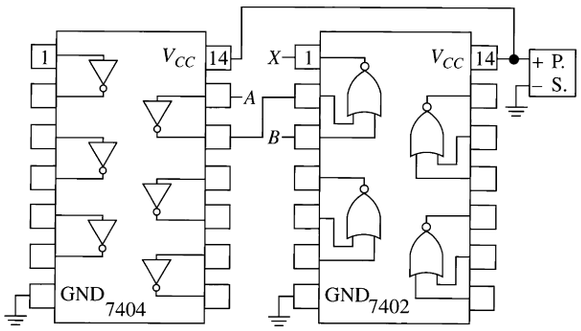
3–38. **(a)** $\overline{A}C$ **(b)** CD **(c)** $\overline{A}CD$ **(d)** $C_P\overline{A}\,\overline{B}$ **(e)** AC **(f)** $C_P AB$

3–39. $U = C_P AB$ $W = BC$
$V = \overline{C}\,\overline{D}$ $X = C_P CD$

3–40.



3–41.



3–42. LOW; to see inverted output pulses (otherwise, output would always be LOW).

3–43. HIGH; to see inverted output pulses (otherwise, output would always be HIGH).

3–44. Pins 4 and 10 should be HIGH. The inverters connected to those pins are bad.

3–45. There is no problem.

3–46. The inverter is not working.

3–47. With all inputs HIGH, pin 8 should be LOW. Next try making each of the 8 inputs LOW, one at a time, while checking for a HIGH at pin 8.

3–48. Pins 8 and 12 should be LOW. The NORs connected to those pins are bad.

3–49. AND − 74HC08; U3:A = location C2, U3:B = location D2 OR − 74HC32; location B7

3–50. **(a)** flashing **(b)** HIGH

3–51. pin 20 = LOW (GND), pin 40 HIGH (+5)

3–52. Because they are all part of one IC package.

3–53. Place probe "A" on the input of the inverter (WATCHDOG_CLK). Using the same settings for probe "B" as "A," place probe "B" on the output of U4:A. "B" should be the complement of "A."

3–54. all HIGH

3–55. OE_B

E3–1. **(a)** $X = 1, Y = 1$
(b) $X = 0, Y = 0$
(c)

A	*B*	*X*
0	0	0
0	1	0
1	0	0
1	1	1

A	*B*	*Y*
0	0	0
0	1	1
1	0	1
1	1	1

E3–2. **(a)** AND
(b) OR

E3–3. **(a)** Up
(b) Down

E3–4. Up ('1')

E3–5. **(a)** Vcc
(b) Logic pulser
(c) Logic probe
(d) Ground
(e) Vcc

E3–6. Password for *Options-Circuit Restrictions Hide component faults* is: **wk5e**
(a) Gates 2 and 3
(b) Gate 3
(c) Gates 1 and 4

E3–7. **(a)** X = 0, Y = 0
(b) X = 1, Y = 1
(c)

A	*B*	*X*
0	0	1
0	1	1
1	0	1
1	1	0

A	*B*	*Y*
0	0	1
0	1	0
1	0	0
1	1	0

E3–8. **(a)** NOR
(b) NAND

E3–9. **(a)** Yes
(b) X = AB
(c) 6mS

E3–10. **(a)** T1 = 6mS, T2 = 10mS, T2 − T1 = 4mS
(b) Two
(c) 1mS

E3–11. **(a)** NAND
(b) NOR

E3–12. **(a)** OR
(b) NAND

E3–13. **(a)** X = C′, D′, Cp
(b) Y = BD′

E3–14. Password for *Options-Circuit Restrictions-Hide component faults* is: **wk5e**
(a) U1b, U1c, are bad
(b) U2c, U2d are bad

E3–15. Password for *Options-Circuit Restrictions-Hide component faults* is: **wk5e**
(a) U1b, U1c, U1d are bad
(b) U2a, U2c are bad

E3–16. Password for *Options-Circuit Restrictions-Hide component faults* is: **wk5e**
(a) U1a, U1c are bad
(b) U2c, U2d are bad

E3–17. Password for *Options-Circuit Restrictions-Hide component faults* is: **wk5e**
(a) U1b, U1c are bad
(b) U2a, U2d are bad

Chapter 4

4–1. The 7400-series uses hard-wired logic. The designer must use a different IC for each logic function. Programmable logic contains thousands of logic gates that can be custom-configured by the designer to perform any logic desired.

4–2. Schematic capture using a CAD system or a Hardware Description Language like VHDL.

4–3. Hardware Description Language

4–4. (1) Define the problem, (2) develop the equations, (3) enter the design, (4) simulate the I/O conditions, (5) program the PLD, (6) test the PLD with actual I/O.

4–5. **(a)** 3, **(b)** 5

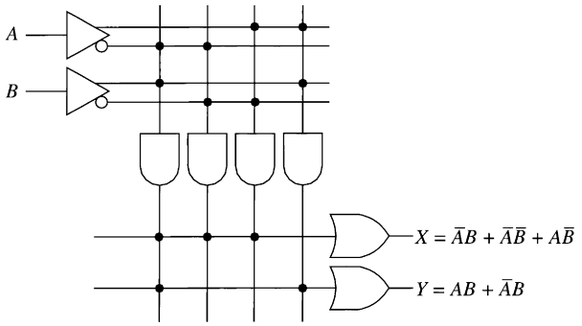
4–6. A small indented circle

4–7. They receive programming information from a PC and program the on-board CPLD that can then be tested with actual I/O signals.

4–8. **(a)** 3
(b) 2
(c) 3

4–9. The PLA provides programmable OR gates for combining the product terms.

4–10.



4–11. So that it won't lose its programmed logic design when power is removed.

4–12. **(a)** 2500 usable gates, 128 macrocells

(b) 2400 usable gates, 108 macrocells

4–13. The look-up table method

4–14.

Inputs		Output
A	*B*	*X*
0	0	1
0	1	0
1	0	1
1	1	0

4–15. They must be re-programmed.

4–16. Schematic entry using a CAD system and VHDL entry using a text editor.

4–17. It translates the information from the design entry stage into a binary file that is later used to program the CPLD.

4–18. It defines the IC pin as an input or output and connects it to the internal CPLD circuitry.

4–19. Text

4–20. **(a)** Library declares which VHDL library to use.

(b) Entity defines the input/output ports.

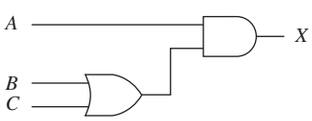
(c) Architecture defines the logic expressions.

4–21.
```
ENTITY and3 IS
PORT(
        A, B, C: IN bit;
        X        :OUT bit);
END and3;
```

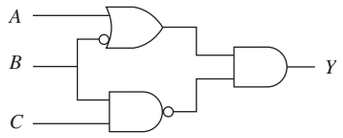
4–22.
```
ARCHITECTURE arc OF and3 IS
BEGIN
        X<=(A AND B AND C);
END arc;
```

4–23.

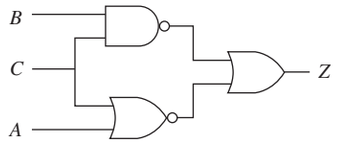
(a)



(b)



(c)



Chapter 5

5–1. $W = (A + B)(C + D)$

$X = AB + BC$

$Y = (AB + B)C$

$Z = (AB + B + (B + C))D$

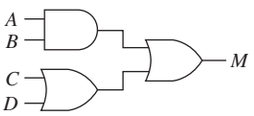
5–2. **(a)** $R = TPF$

(b) $G = TP(M + F)$

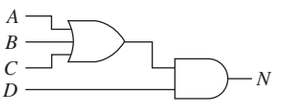
(c) $B = F(H + T + P)$

5–3.

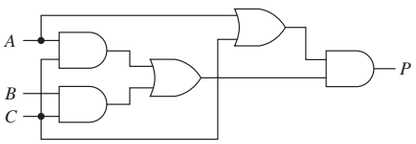
(a)



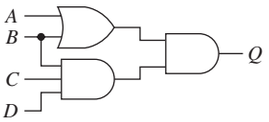
(b)



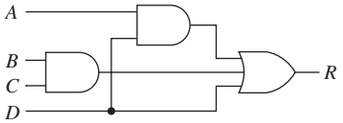
(c)



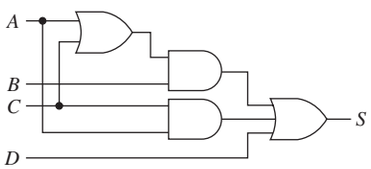
(d)



(e)



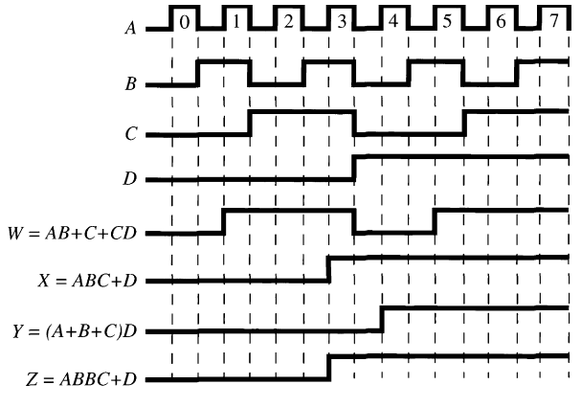
(f)



A	B	C	D	M	N	Q	R	S
0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	1	1
0	0	1	0	1	0	0	0	0
0	0	1	1	1	1	0	1	1
0	1	0	0	0	0	0	0	0
0	1	0	1	1	1	0	1	1
0	1	1	0	1	0	0	1	1
0	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1	1
1	0	1	0	1	0	0	0	1
1	0	1	1	1	1	0	1	1
1	1	0	0	1	0	0	0	1
1	1	0	1	1	1	0	1	1
1	1	1	0	1	0	0	1	1
1	1	1	1	1	1	1	1	1

A	B	C	P
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

5–4.



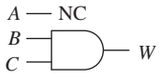
5–5. **(a)** Commutative law **(b)** Associative law
(c) Distributive law

5–6.

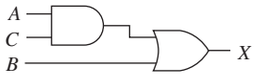
$M = O$	$S = 0$
$N = 1$	$T = A$
$P = AB$	$U = 1$
$Q = C + D$	$V = A$
$R = A$	$W = A$

5–7.

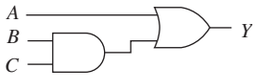
$W = (A + B)BC$
$W = BC$



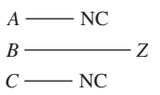
$X = (A + B)(B + C)$
$X = B + AC$



$Y = A + (A + B)BC$
$Y = A + BC$

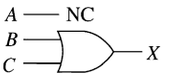


$Z = AB + B + BC$
$Z = B$

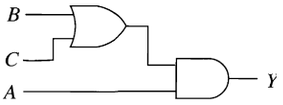


5–8.

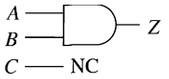
$X = (A + B)(B + C) + B + C$
$X = B + C$



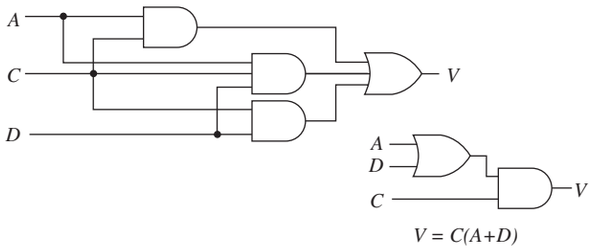
$Y = (A + B)(B + C)A$
$Y = A(B + C)$



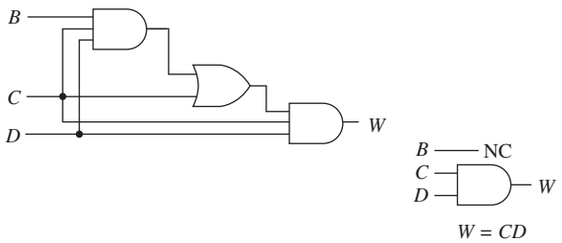
$Z = AB + AB(B + C)$
$Z = AB$



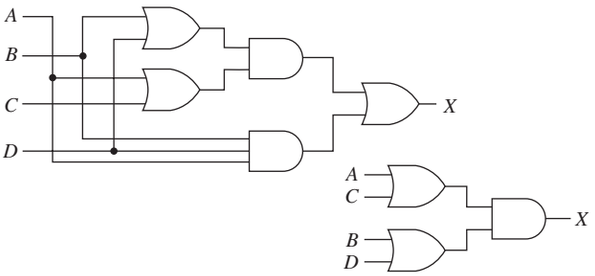
5–9.



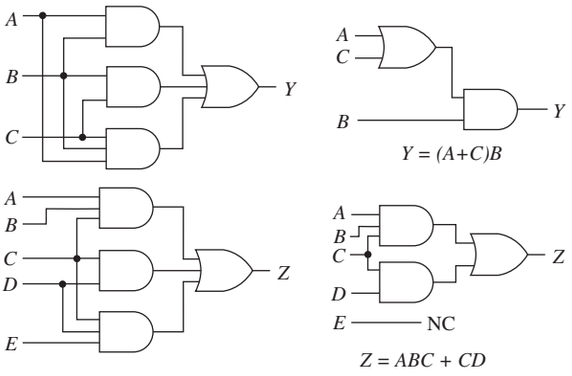
$V = C(A+D)$



$W = CD$



$X = (A+C)(B+D)$



5–10.

A	C	D	V
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

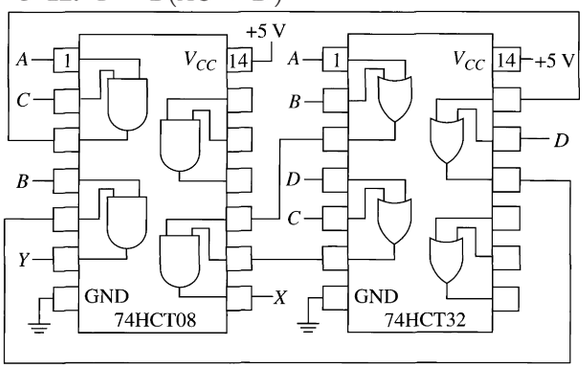
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

A	B	C	D	X	Z
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	1	1	1
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	1	1
1	1	1	1	1	1

C	D	W
0	0	0
0	1	0
1	0	0
1	1	1

5–11. $X = (A + B)(D + C)$

5–12. $Y = B(AC + D)$



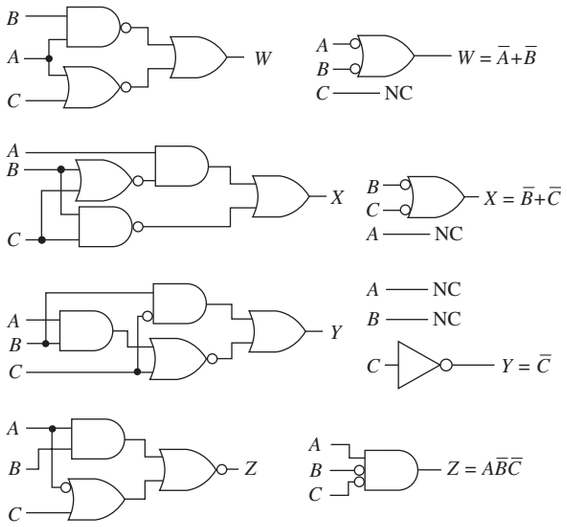
5–13. Break the long bar and change the AND to an OR, or the OR to an AND.

5–14. **(a)** NAND **(b)** NOR

5–15. Y and Z are both ORs.

5–16. $\overline{\overline{A} + \overline{B}} = \overline{\overline{A}}\,\overline{\overline{B}} = AB$

5–17.



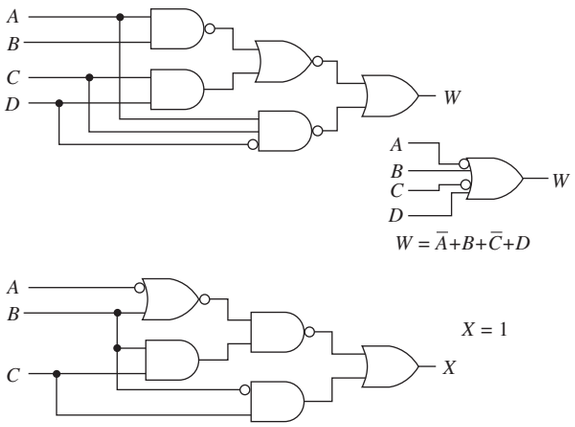
5–18. **(a)** $X = \overline{\overline{AB} + (B + C)}$

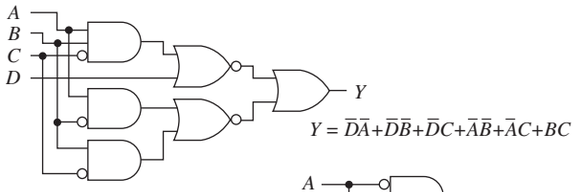
$X = 0$

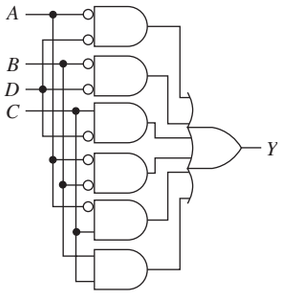
(b) $Y = \overline{\overline{A} + \overline{B}BC}$

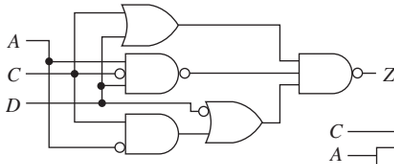
$Y = 1$

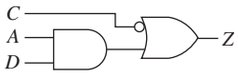
5–19.











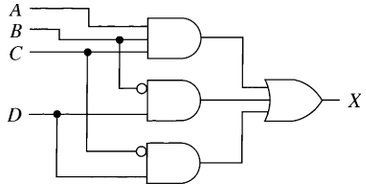
$Z = \overline{C}+AD$

5–20. **(a)** $X = \overline{(\overline{A} + \overline{B}) + \overline{BC}} + \overline{B}\overline{C}D$

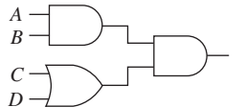
$X = \overline{ABC + \overline{B}D + \overline{C}D}$

(b) $Y = \overline{A}B + \overline{A}BC \cdot (\overline{B} + \overline{C})$

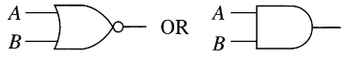
$Y = 1$



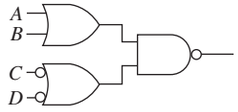
5–21.



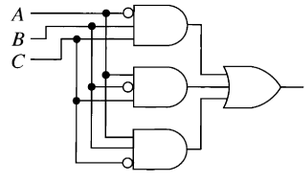
5–22.



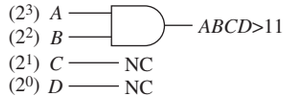
5–23.



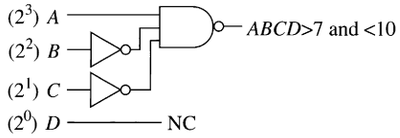
5–24.



5–25.



5–26.

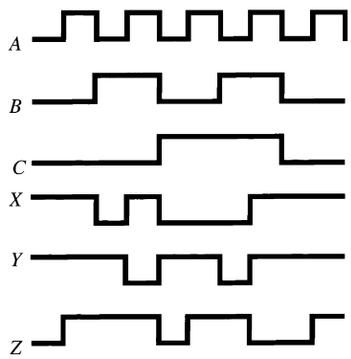


5–27.

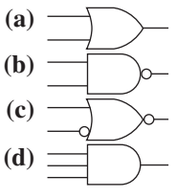
A	B	C	W	X
0	0	0	0	1
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	0	1
1	1	1	0	0

A	B	C	D	Y	Z
0	0	0	0	1	1
0	0	0	1	1	1
0	0	1	0	1	1
0	0	1	1	0	1
0	1	0	0	0	0
0	1	0	1	1	0
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	1	0	0
1	1	0	0	0	0
1	1	0	1	1	0
1	1	1	0	0	1
1	1	1	1	1	0

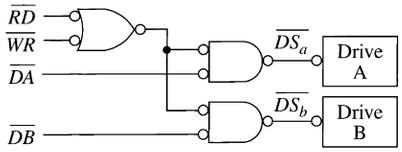
5–28.



5–29.

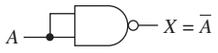


5–30.

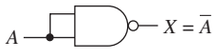


5–31.

(a)

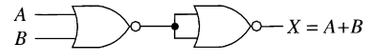


(b)

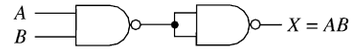


5–32.

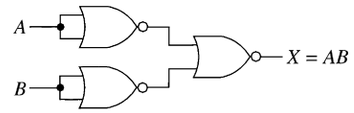
(a)



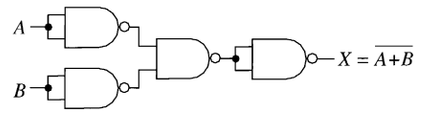
(b)



(c)

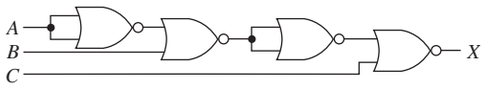


(d)

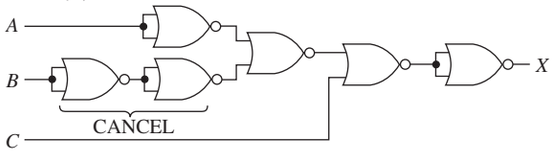


5–33.

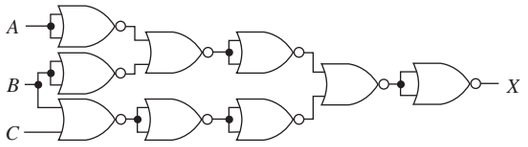
(a)



(b)

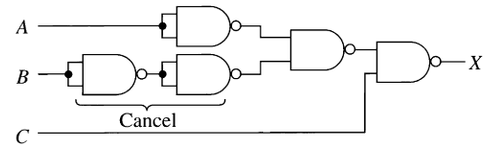


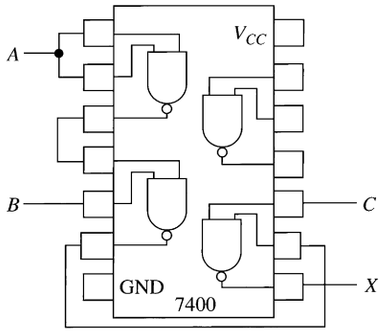
(c)



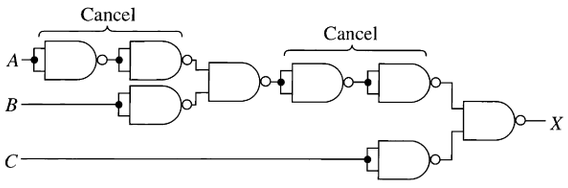
5–34.

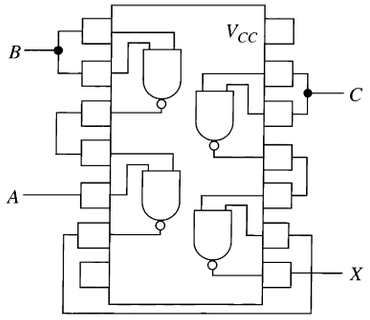
(a)





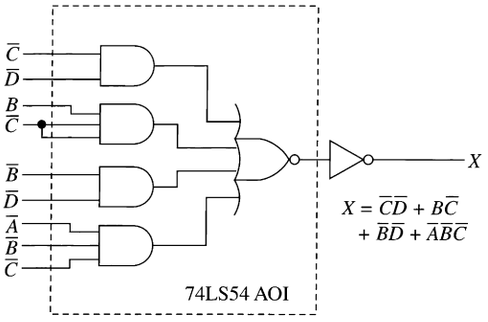
(b)





5–35. u. SOP
v. POS
w. POS
x. SOP
y. POS
z. POS, SOP

5–36.

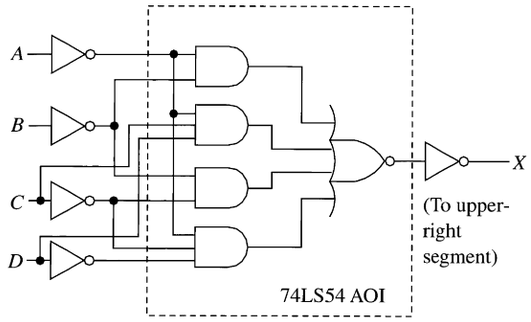


5–37. $X = \overline{A} + B\overline{C}$
$Y = B + \overline{A}C$
$Z = A\overline{C} + AB + \overline{A}\,\overline{B}\,C$

5–38. $W = \overline{B}\,\overline{C} + \overline{B}\,\overline{D} + \overline{A}\,\overline{B}$
$X = \overline{C}\,\overline{D} + \overline{B}\,\overline{D} + ABCD$
$Y = A\overline{B} + A\overline{D} + \overline{B}C\overline{D}$
$Z = \overline{C} + B\overline{D} + \overline{A}\,\overline{D}$

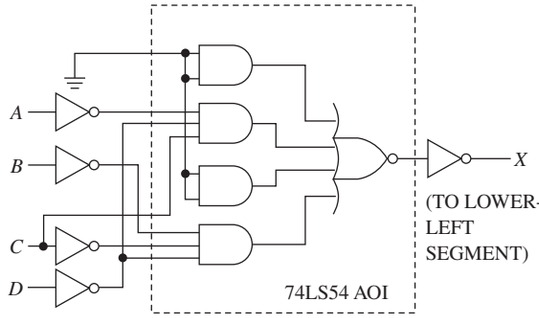
5–39. **(a)** $X = \overline{C}D + AC + B$
(b) $Y = 1$

5–40.



$X = \overline{A}\overline{B} + \overline{A}CD + \overline{B}\overline{C} + \overline{A}\overline{C}\overline{D}$ where A = MSB

5–41.



$X = \overline{A}C\overline{D} + \overline{B}\overline{C}\overline{D}$ where A = MSB

5–42. Pin 6 should be ON; bad gate.

5–43. The IC checks out OK. The problem is that pin 9 should be connected to pin 10 (not 9 to GND).

5–44. The output (pin 8) would be stuck high.

5–45. $\overline{\text{WATCHDOG\_EN} \cdot \text{Qa}}$

5–46. $\overline{\text{WATCHDOG\_EN} \cdot \text{Qa}} + \text{Qb}$

5–47. **(a)** pin 6 = $\overline{\overline{\text{P1.0}} + \overline{\text{A15}}}$ **(b)** AND
(c) quad 2 input AND
(d) $\overline{\text{RD}}$ is LOW or $\overline{\text{WR}}$ is LOW

5–48. Pin 20 of U10 goes LOW if RESET and A15 are both LOW.

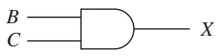
E5–1. **(a)** B = KD + HD
(b) B = D(K + H)

E5–2. **(a)** Seven
(b) X = AB + BC

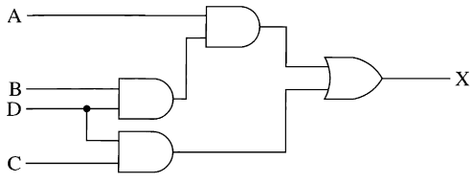
E5–3. **(a)** 5
(b) X = BC + A

E5–4. **(a)** X = (A + B)(B + C) + (B + C)
(b) Six
(c) X = B + C

E5–5. **(a)** 2
(b) X = BC
(c)



E5–6. **(a)** Ten
(b) X = ABD + CD
(c)



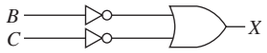
E5–7. X = AB′C′ + A′BC′ + AB′C

E5–8. X = A′BC′ + AB′C + A′BC + ABC

E5–9. **(a)** 2
(b) X = B′C′

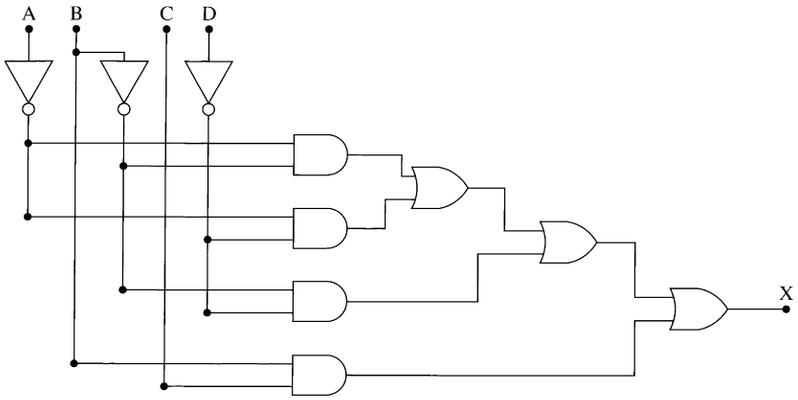
E5–10. **(a)** X = $((A + B)'(B + C))'$
(b) 7
(c) X = A + C′ + B

E5–11. **(a)** 6
(b) X = B′ + C′
(c)



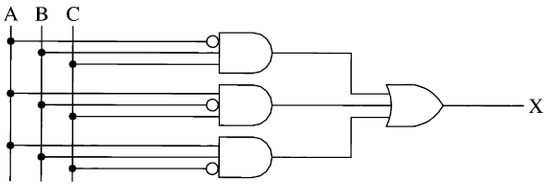
E5–12. **(a)** 11
(b) X = A′B′ + A′D′ + B′D′ + BC

(c)

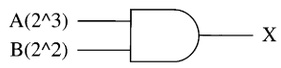


E5–13. **(a)** AND
(b) OR

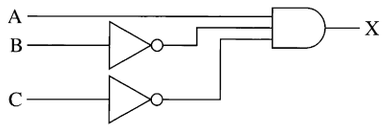
E5–14.



E5–15.



E5–16.



E5–17. Password for *Options-Circuit Restrictions-Hide component faults* is: **wk5e**

(a) U1b is bad **(b)** U1a is bad

E5–18. Password for *Options-Circuit Restrictions-Hide component faults* is: **wk5e**

(a) U1a is bad **(b)** U1b is bad

E5–19. Password for *Options-Circuit Restrictions-Hide component faults* is: **wk5e**

(a) U2b is bad **(b)** U3a is bad

E5–20. Password for *Options-Circuit Restrictions-Hide component faults* is: **wk5e**

(a) U2b is bad **(b)** U1b is bad

E5–21. Password for *Options-Circuit Restrictions-Hide component faults* is: **wk5e**

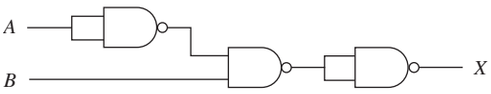
(a) U1a is bad **(b)** U2a is bad

E5–22. Password for *Options-Circuit Restrictions-Hide component faults* is: **wk5e**

(a) U3a is bad **(b)** U2a is bad

E5–23. Password for *Options-Circuit Restrictions-Hide Component faults* is: **wk5e**

(a) 3
(b) Gate 2
(c)



E5–24. Password for *Options-Circuit Restrictions-Hide Component faults* is: **wk5e**

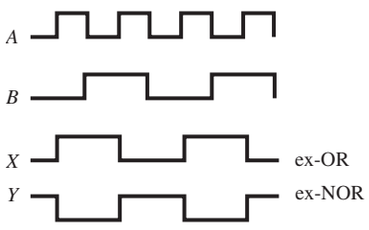
(a) $X = (A'B')'$
(b) $X = A + B$
(c) No
(d) Yes, Gate 1

Chapter 6

6–1. **(a)** Exclusive-OR produces a HIGH output for one or the other input HIGH, but not both.
(b) Exclusive-NOR produces a HIGH output for both inputs HIGH or both inputs LOW.

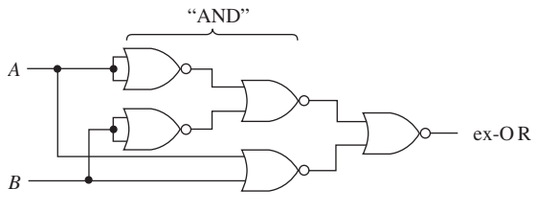
6–2. **(a)** An OR outputs a HIGH for both inputs HIGH.
(b) An AND outputs a LOW for both inputs LOW.

6–3.

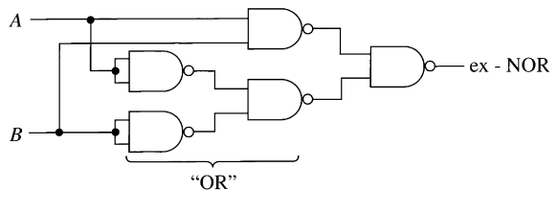


6–4. $W = \overline{\overline{AB} \cdot A + B} = AB + \overline{A}\,\overline{B}$ (ex-NOR)
$X = AB + \overline{A + B} = AB + \overline{A}\,\overline{B}$ (ex-NOR)
$Y = \overline{AB} \cdot \overline{\overline{AB}} = \overline{AB} + A\overline{B}$ (ex-OR)
$Z = \overline{\overline{AB} + \overline{A + B}} = AB$ (neither)

6–5.



6–6.



6–7. $X = \overline{(AB + \overline{A}\,\overline{B}) + \overline{A}\overline{B}} = A\overline{B}$

$Y = \overline{\overline{A}B + A\overline{B} \cdot AB} = 1$

6–8. $X = \overline{A}\overline{B}BC + \overline{\overline{A}B}\,\overline{BC}$

$X = \overline{A}BC + AB\overline{C}$

$Y = \overline{\overline{AB + C}\,\overline{AB} + \overline{\overline{AB + C}}\,AB}$

$Y = \overline{C} + AB$

6–9. A7 = 1010 0111 0

4C = 0100 1100 0

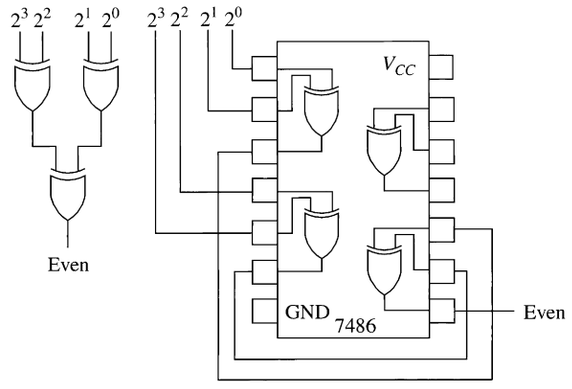
79 = 0111 1001 0

F3 = 1111 0011 1

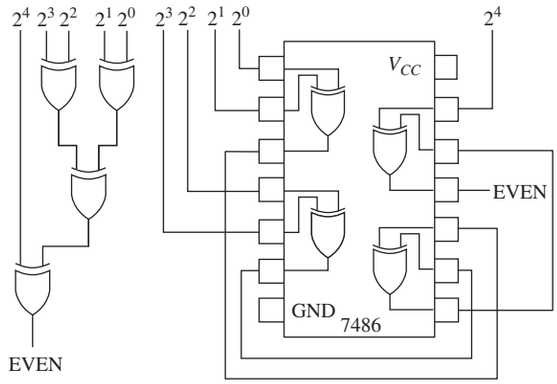
00 = 0000 0000 1

FF = 1111 1111 1

6–10.

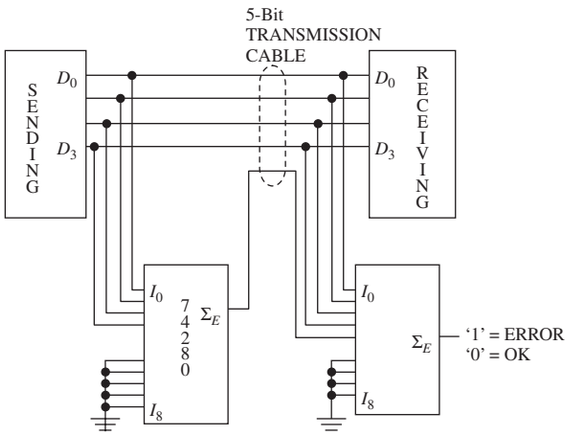


6–11.

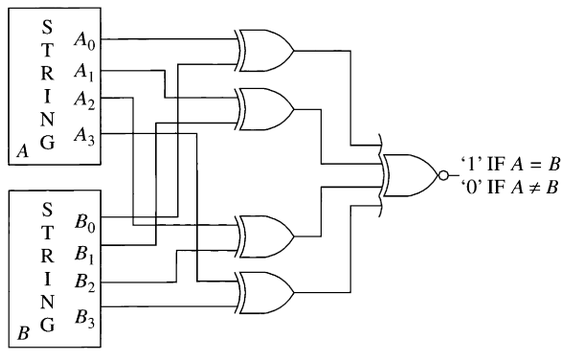


6–12. Odd

6–13.



6–14.



6–15. Yes; LOW