

**Gregory L. Moss**

**Lab Solutions Manual**

**for**

**Lab Manual: A Design Approach**

to accompany

**DIGITAL SYSTEMS:**

**PRINCIPLES AND APPLICATIONS**

Eleventh Edition

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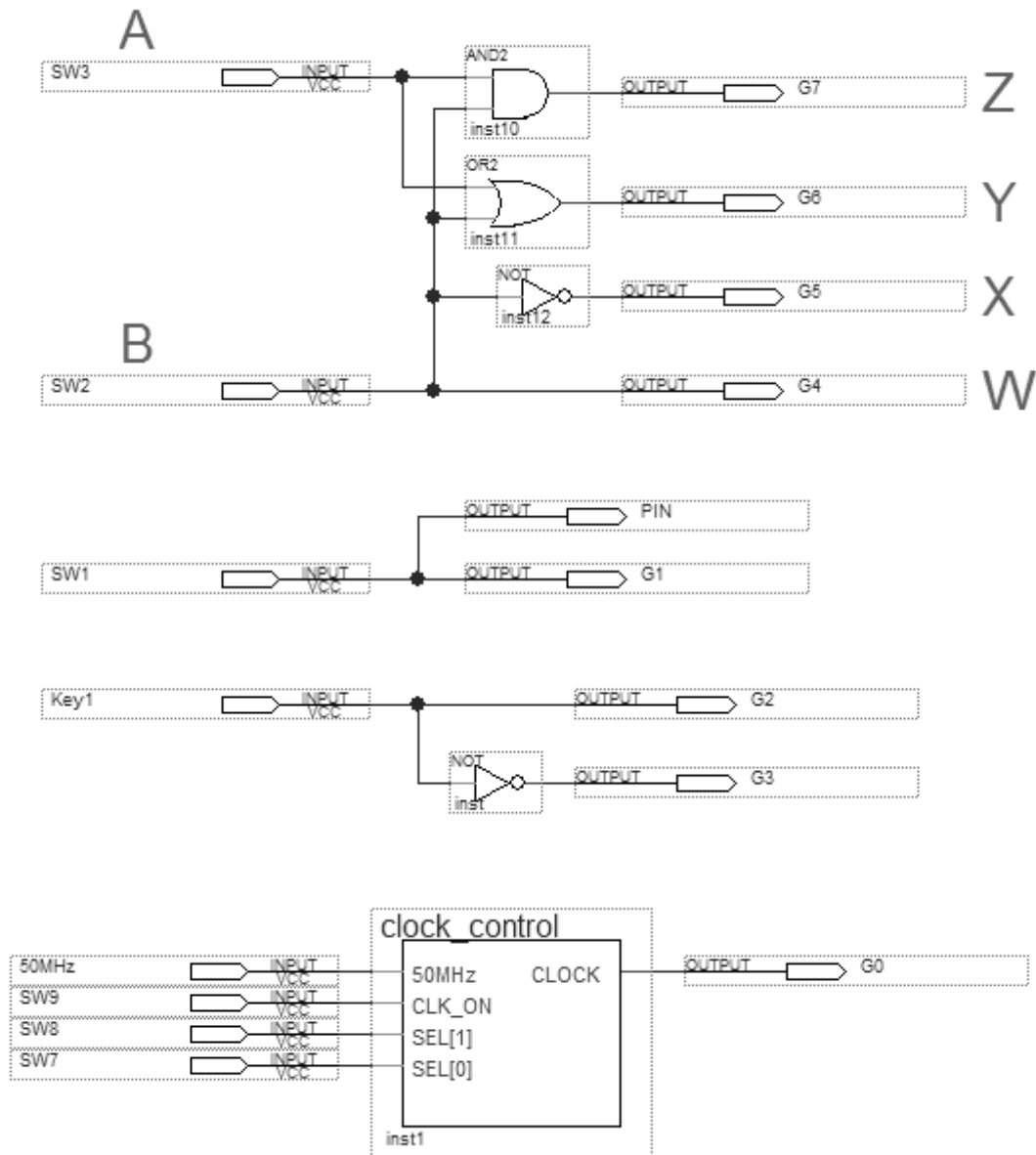
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## Unit 1 Introduction to the DE0, DE1, or DE2 Development & Education Board

Project: Intro2DE0, Intro2DE1, or Intro2DE2



### 1.3 Logic Switches

Board	DE0	DE1	DE2
# switches	10	10	18

Logic Switch SW1	LEDG1 (on/off)	Logic level (high/low)	Voltage at connector pin
Down	Off	Low	~0 V
Up	On	High	~3.3 V

#### 1.4 LEDs

LED label	Color	DE0	DE1	DE2
LEDR	Red	0	10	18
LEDG	Green	10	8	9

#### 1.5 Pushbuttons → Normally High

Board	DE0	DE1	DE2
Pushbutton	3	4	4

Pushbutton #1	LEDG2 (on/off)	LEDG3 (on/off)
Normal	On	Off
Pressed	Off	On

#### 1.6 Clock

CLK_ON (SW9)	1	1	1	1	0
SEL[1..0] (SW8, SW7)	00	01	10	11	XX
freq <sub>G0</sub>	0.5 Hz	5 Hz	25 Hz	50 Hz	0 Hz

#### 1.7 Simple logic circuits

A (SW3)	B (SW2)	W (LEDG4)	X (LEDG5)	Y (LEDG6)	Z (LEDG7)
0	0	0	1	0	0
0	1	1	0	1	0
1	0	0	1	1	0
1	1	1	0	1	1

$$W = B$$

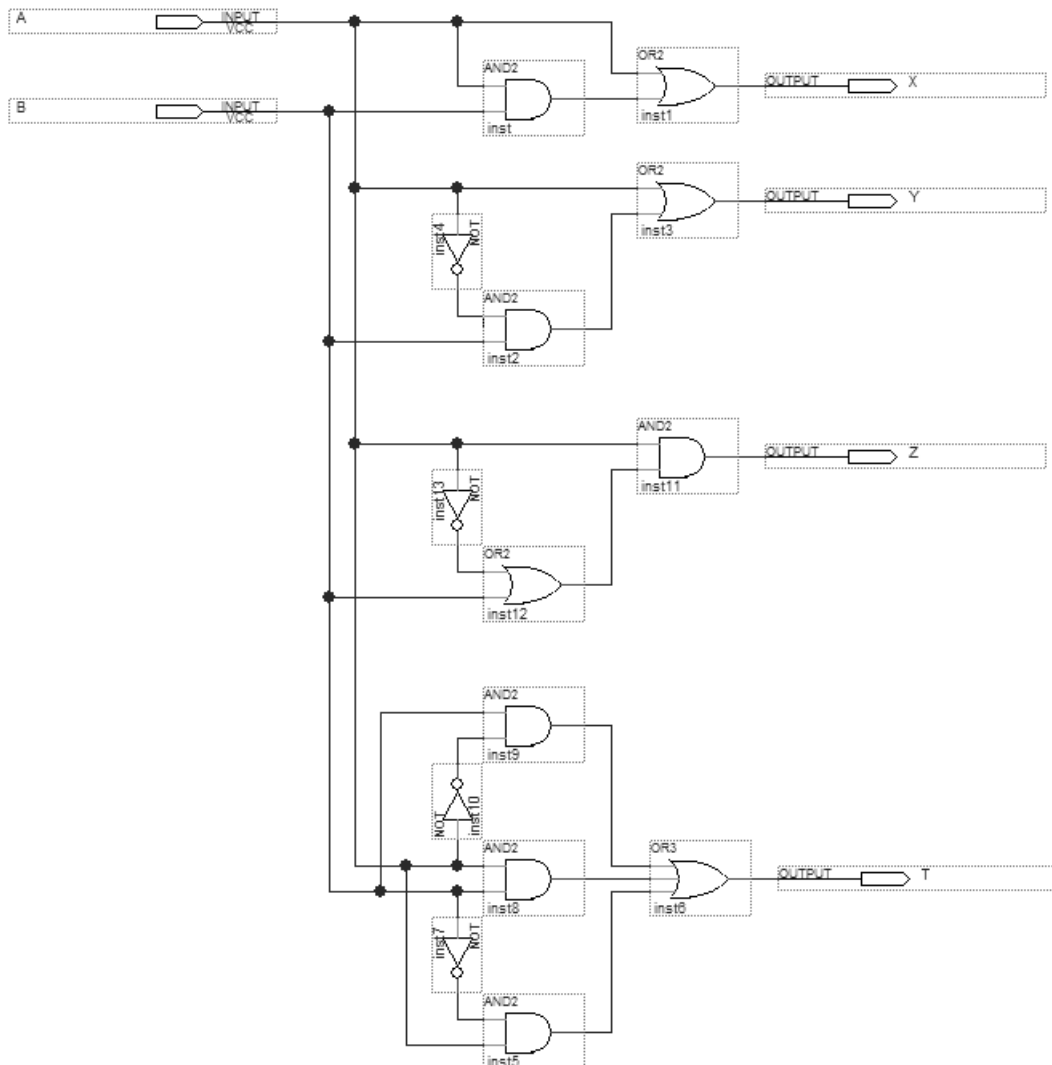
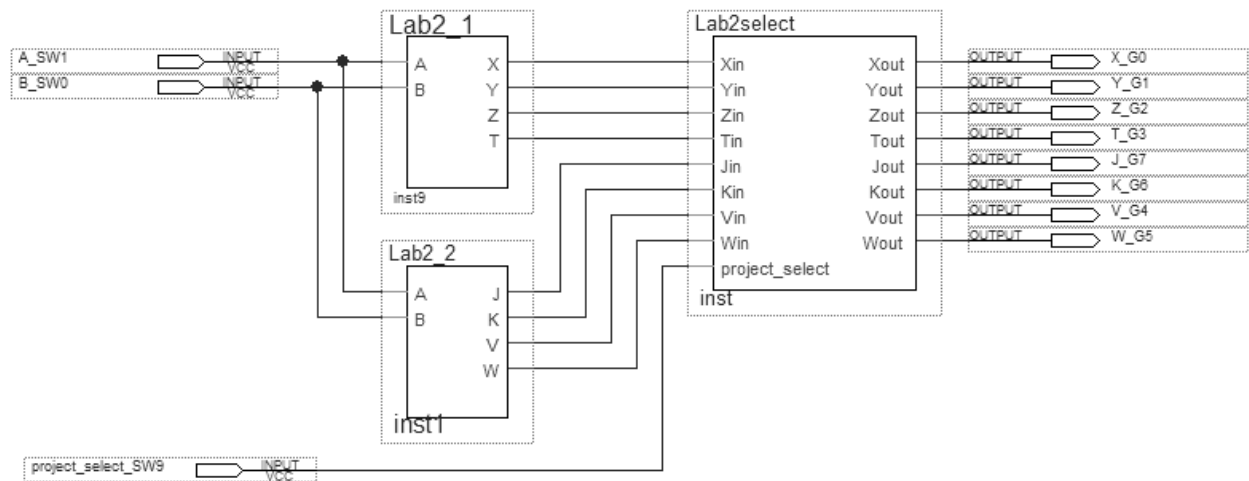
$$X = \overline{B}$$

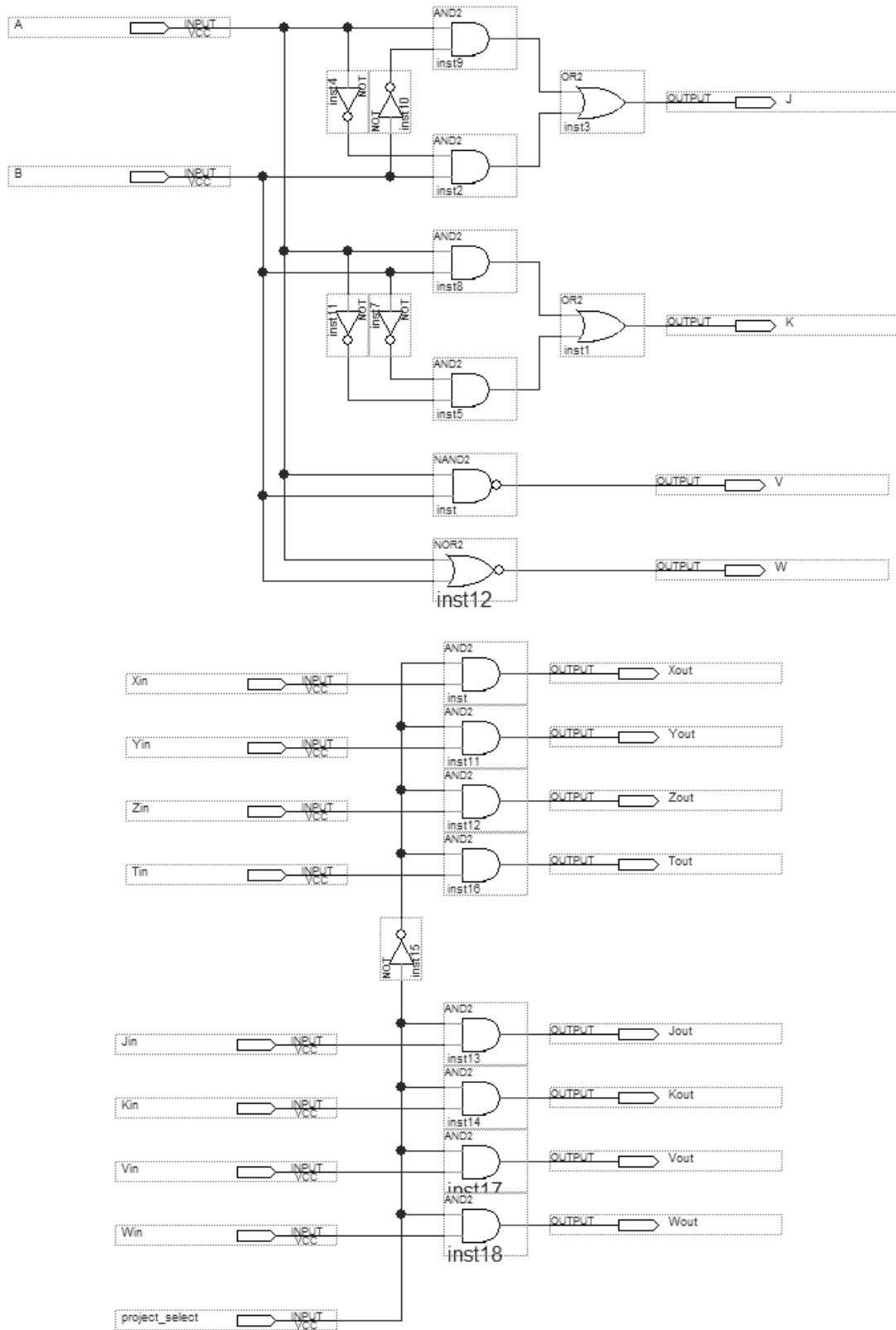
$$Y = A + B$$

$$Z = A \cdot B$$

## Unit 2 Testing Combinational Logic Circuits Using DE0, DE1, or DE2 Boards

Project: Lab2DE0, Lab2DE1, or Lab2DE2





## 2.1 Simple circuits

$$X = A + A B = A$$

$$Y = A + \bar{A} B = A + B$$

$$Z = A (\bar{A} + B) = A B$$

$$T = \bar{A} B + A B + A \bar{B} = A + B$$

A	B	T	Z	Y	X	J	K	W	V
0	0	0	0	0	0	0	1	1	1
0	1	1	0	1	0	1	0	0	1
1	0	1	0	1	1	1	0	0	1
1	1	1	1	1	1	0	1	0	0

## 2.2 More circuit functions

$$V = \overline{A B}$$

$$W = \overline{A + B}$$

$$J = A \bar{B} + \bar{A} B = A \oplus B$$

$$K = A B + \bar{A} \bar{B} = \overline{A \oplus B}$$



### Unit 3 Schematic Capture & Analysis of Combinational Logic Circuits

3.1 Example 3-1 (see Lab Manual Example 3-1 & Quartus Tutorial 1 – Schematic)

3.2 Equivalent circuits

(a)  $V = W?$  true

$$V = A (B + C)$$

$$W = A C + A B$$

(b)  $X = Y?$  true

$$X = \bar{A} \bar{B} + A B + A C$$

$$Y = \bar{A} \bar{B} + A B + \bar{B} C$$

A	B	C	V	W	X	Y
0	0	0	0	0	1	1
0	0	1	0	0	1	1
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	0	0	0
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

3.3 DeMorgan's theorem

(a)  $p1 = p2 = p3?$  true

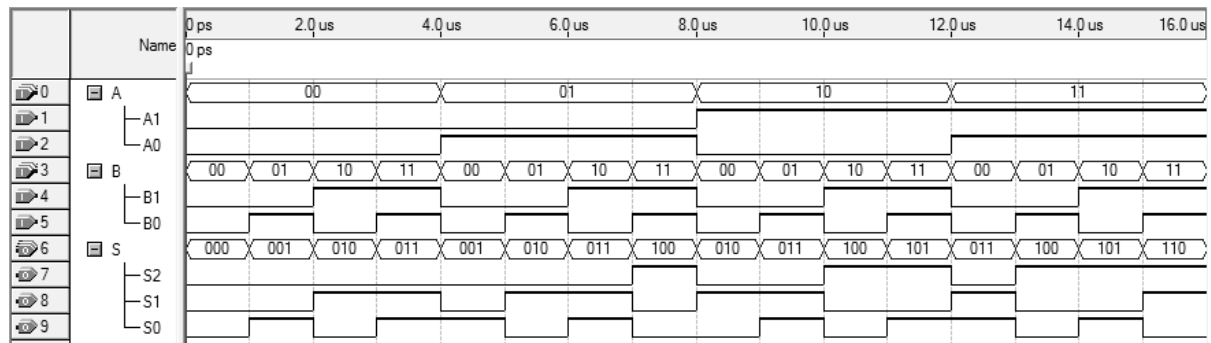
$$p1 = \bar{a} \bar{b} \quad p2 = \bar{a} \bar{b} \quad p3 = \overline{a + b}$$

(b)  $q1 = q2 = q3?$  true

$$q1 = \bar{a} + \bar{b} \quad q2 = \bar{a} + \bar{b} \quad q3 = \overline{a b}$$

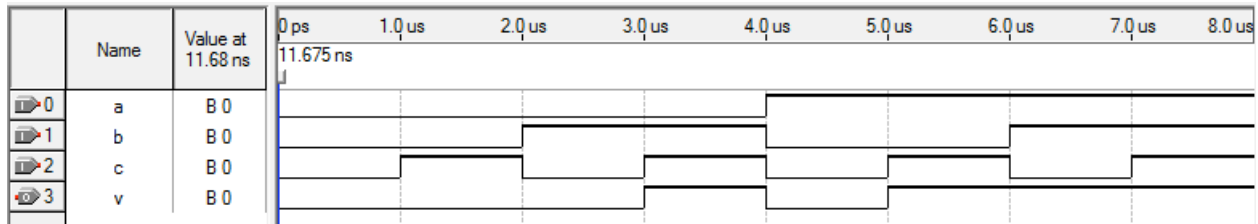
a	b	p	q
0	0	1	1
0	1	0	1
1	0	0	1
1	1	0	0

### 3.4 2-bit adder



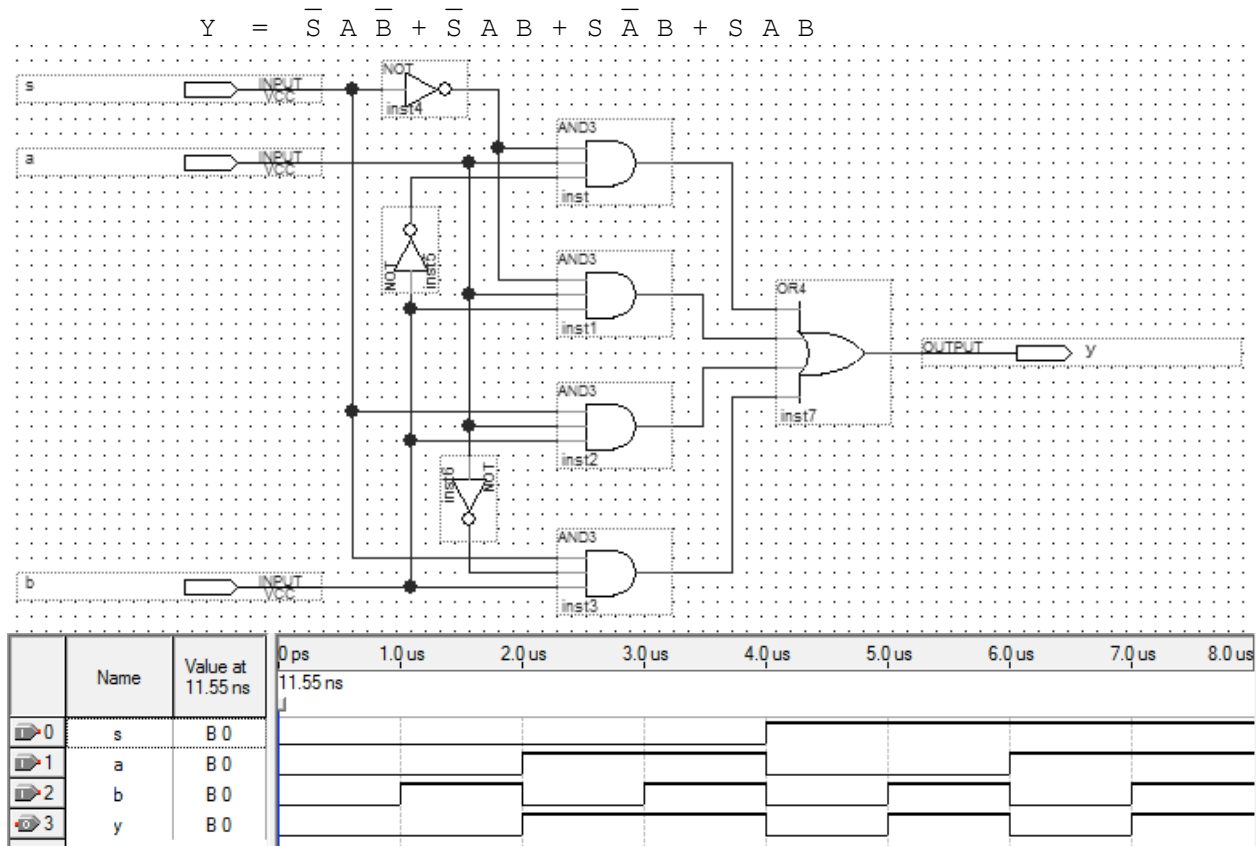
## Unit 4 Design and Simulation of Combinational Circuits

### 4.1 Majority vote (see Lab Manual Example 4-1 & Quartus Tutorial 2 – Simulation)



### 4.2 Two-input multiplexer

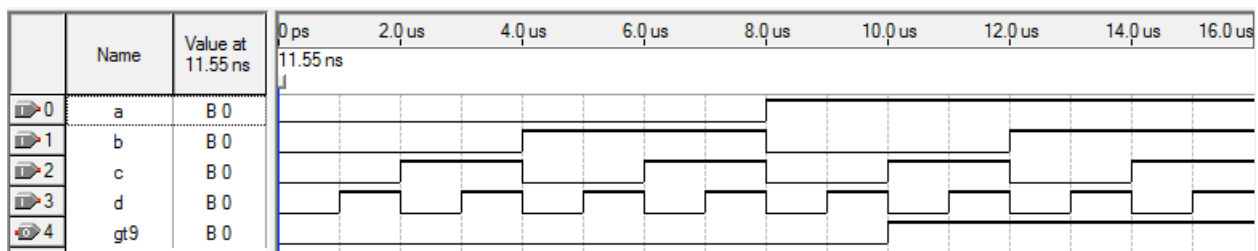
S	A	B	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

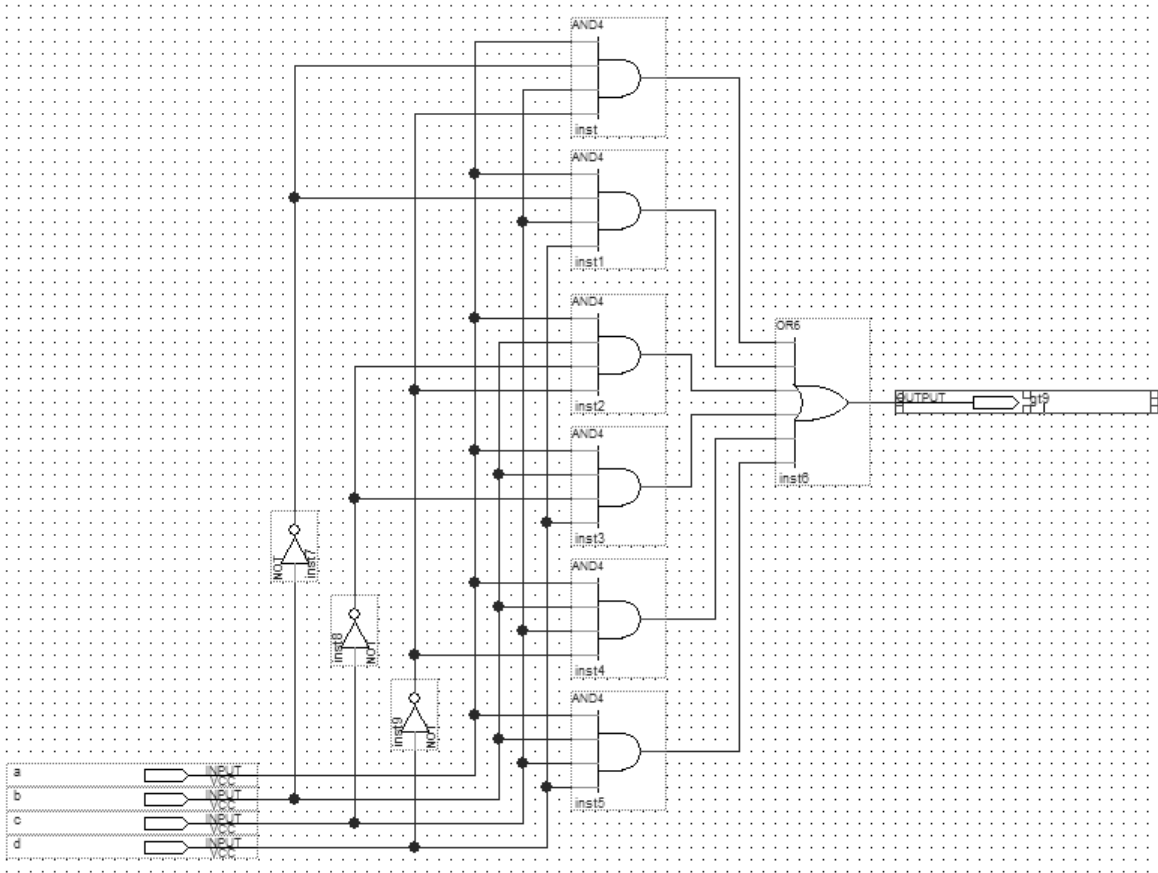


### 4.3 Non-BCD input

A	B	C	D	GT9
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

$$\begin{aligned}
 GT9 = & A \bar{B} C \bar{D} + A \bar{B} C D + A B \bar{C} \bar{D} + A B \bar{C} D \\
 & + A B C \bar{D} + A B C D
 \end{aligned}$$

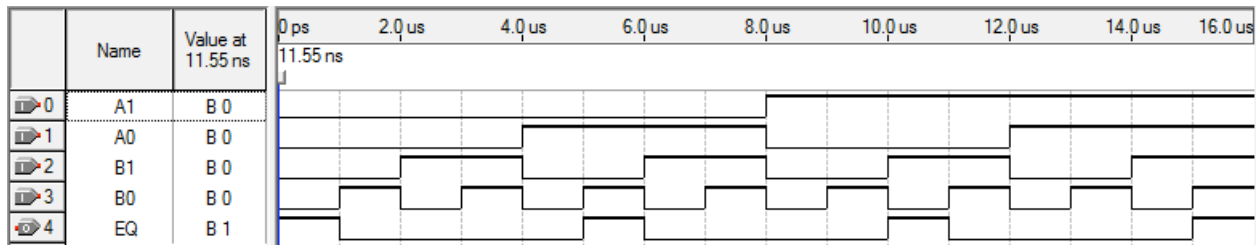
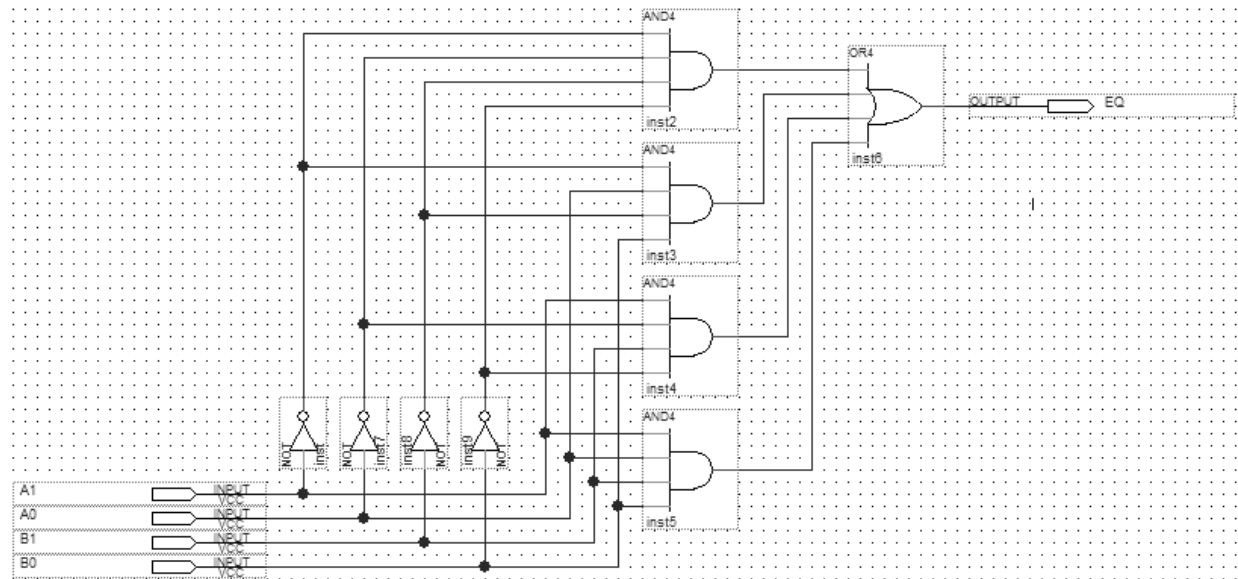




#### 4.4 Two-bit comparator

A1	A0	B1	B0	EQ
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

$$EQ = \overline{A1} \overline{A0} \overline{B1} \overline{B0} + \overline{A1} A0 \overline{B1} B0 + A1 \overline{A0} B1 \overline{B0} + A1 A0 B1 B0$$



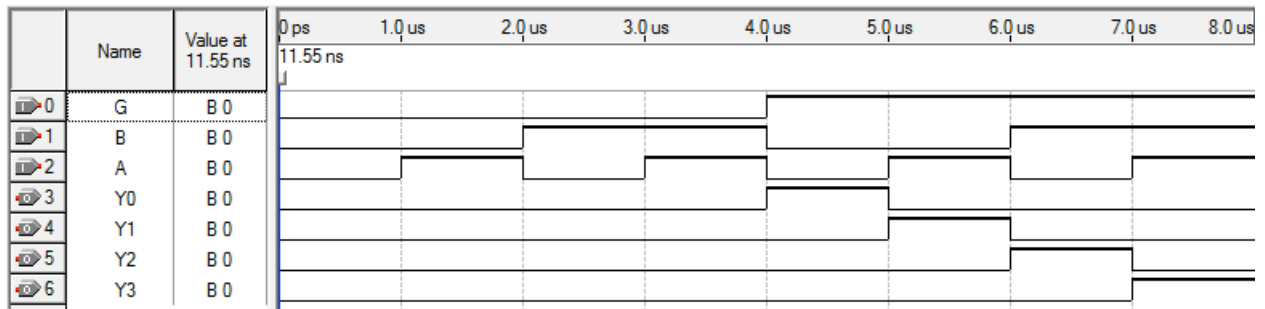
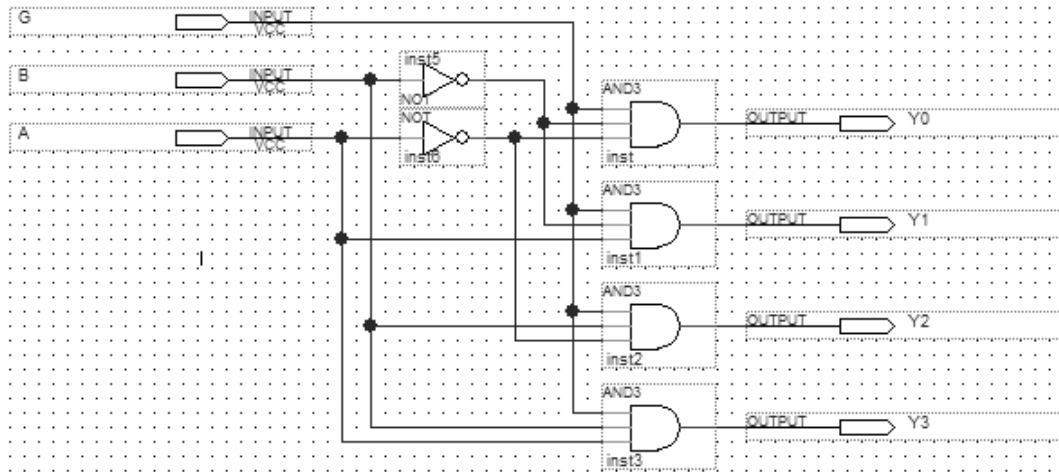
#### 4.5 Binary number detector

$$Y0 = G \bar{B} \bar{A}$$

$$Y1 = G \bar{B} A$$

$$Y2 = G B \bar{A}$$

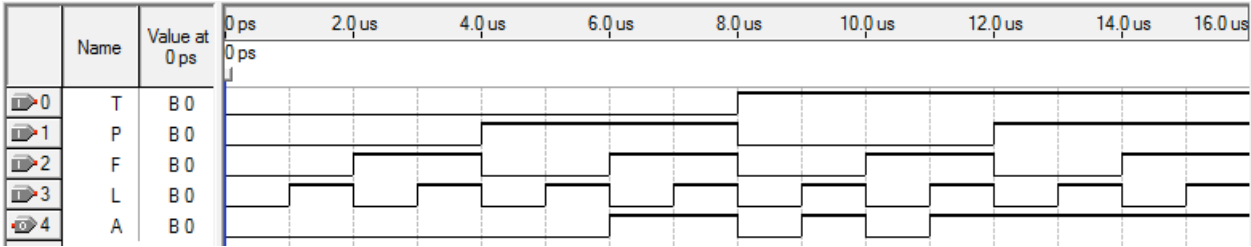
$$Y3 = G B A$$



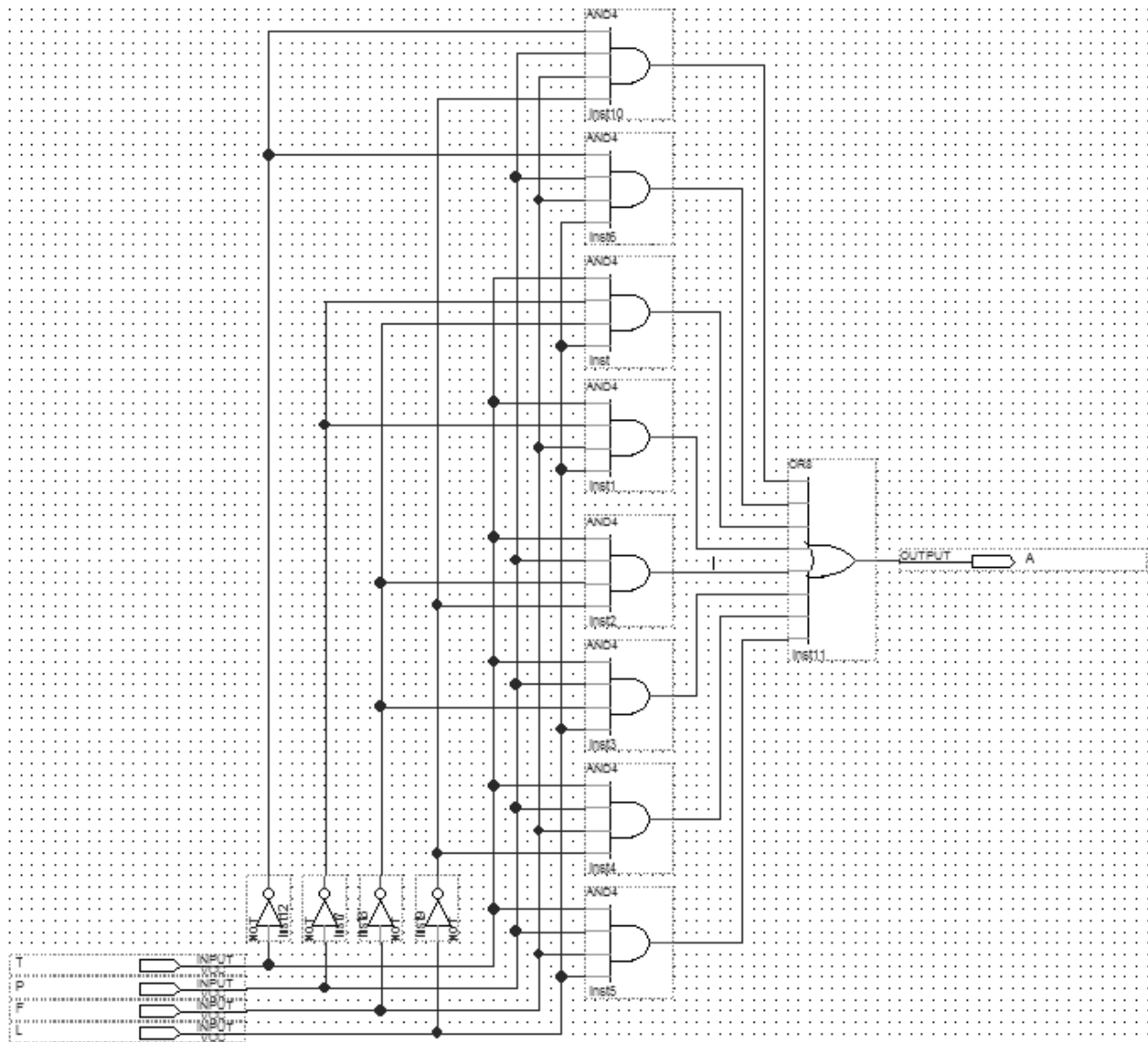
4.6 Alarm circuit

T	P	F	L	A
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

$$A = \overline{T} P F \overline{L} + \overline{T} P F L + T \overline{P} \overline{F} L + T \overline{P} F L$$
$$+ T P \overline{F} \overline{L} + T P \overline{F} L + T P F \overline{L} + T P F L$$



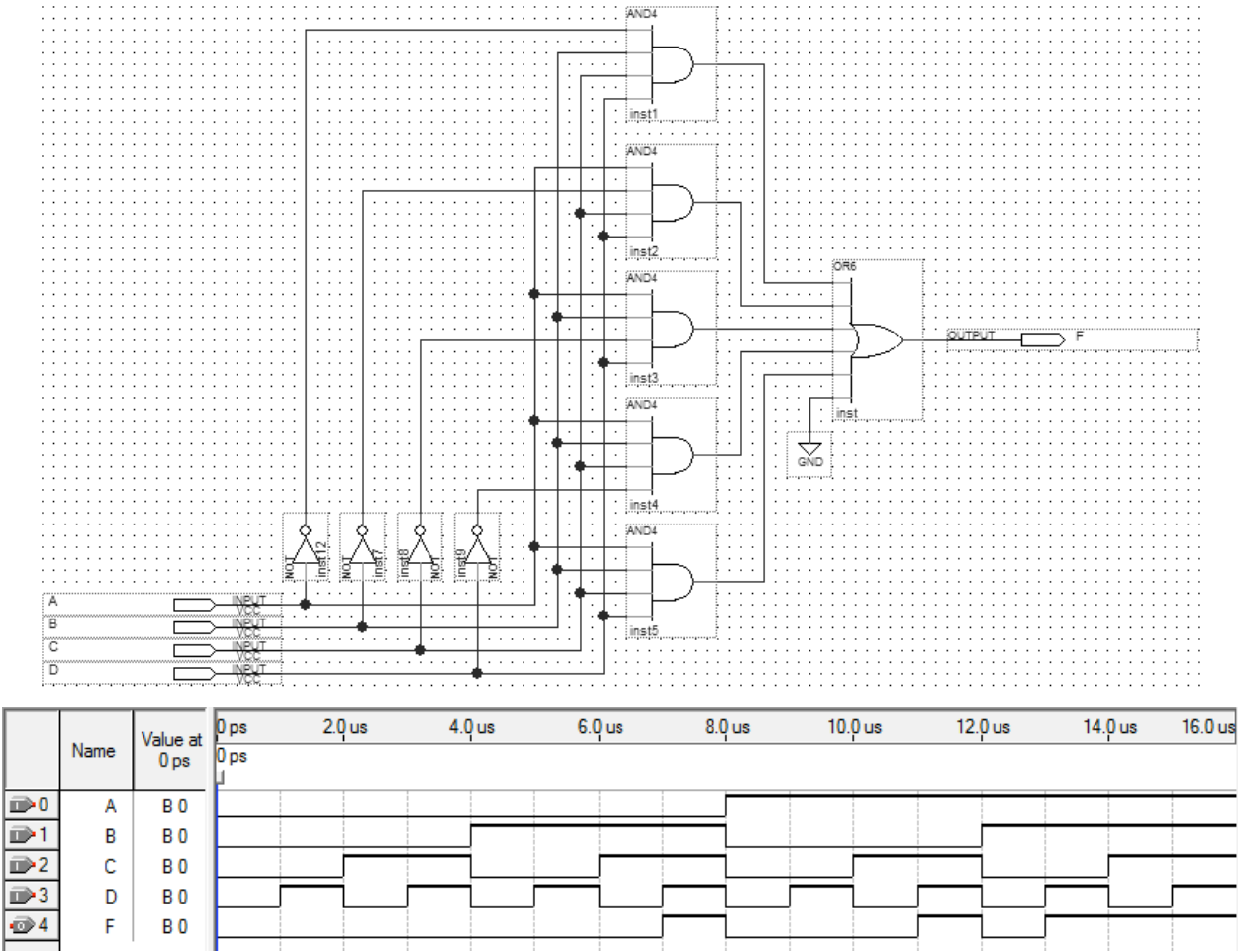




4.7 Elevator control

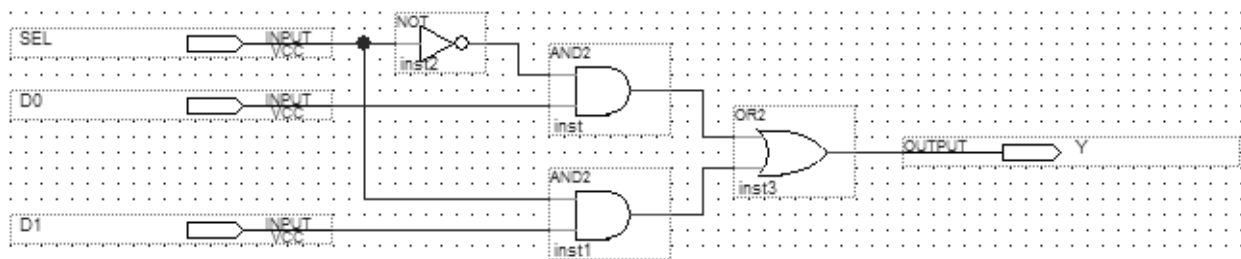
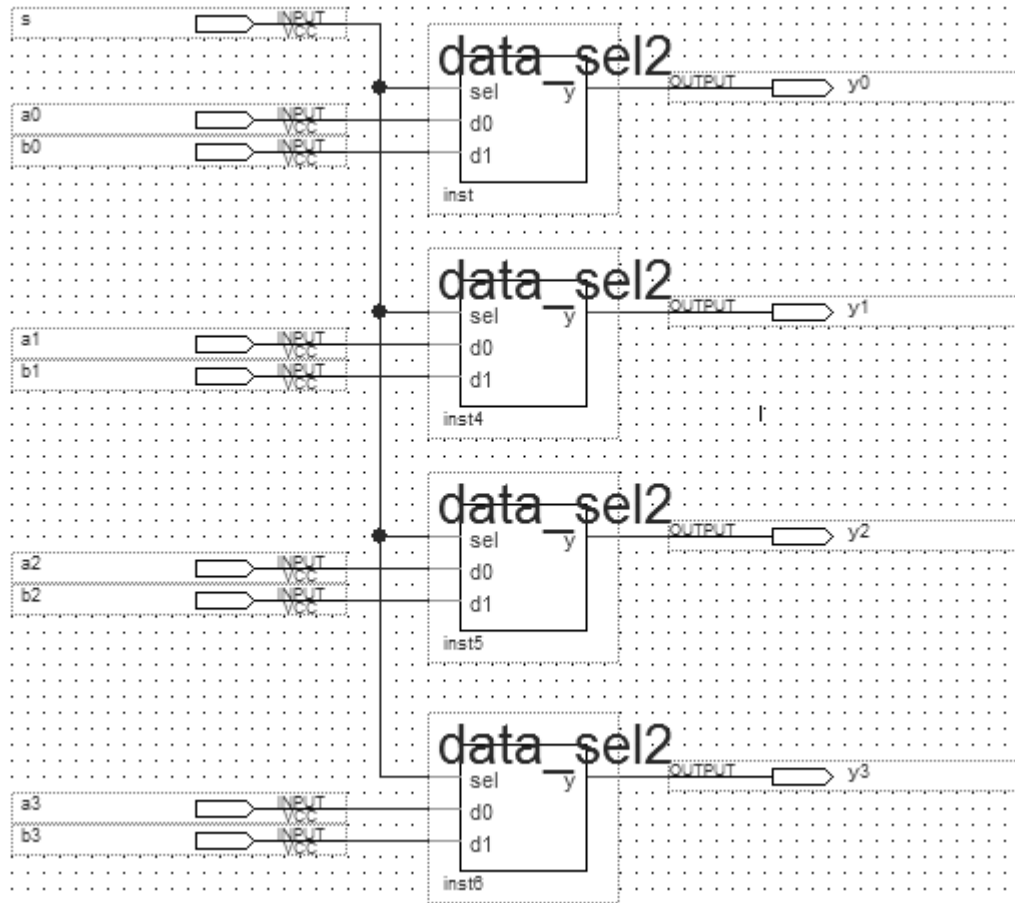
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

$$F = \bar{A} B C D + A \bar{B} C D + A B \bar{C} D + A B C \bar{D} + A B C D$$

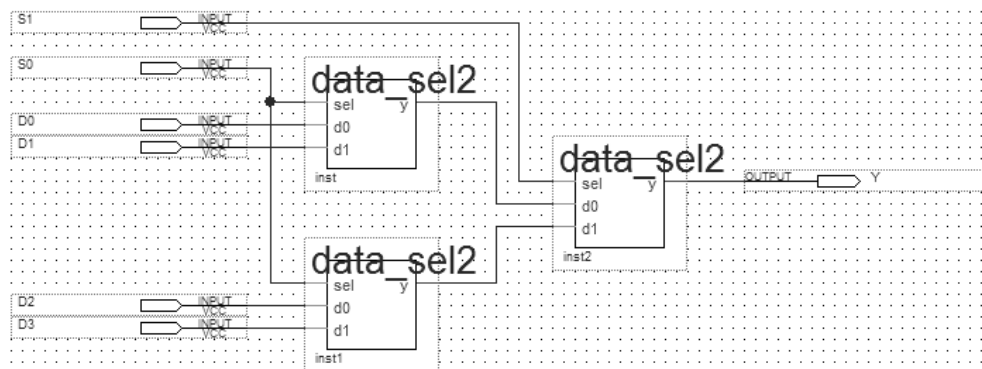
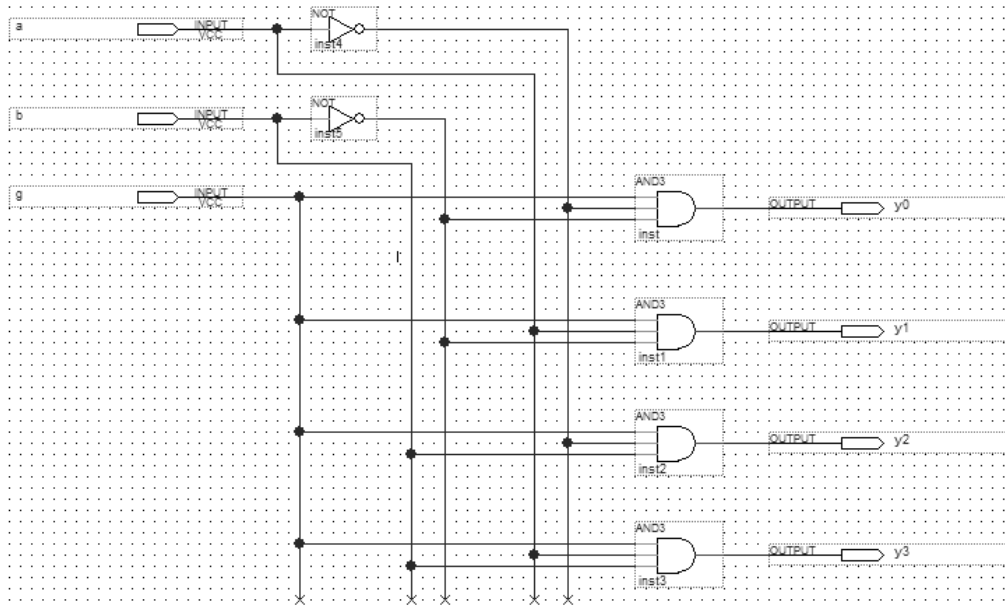
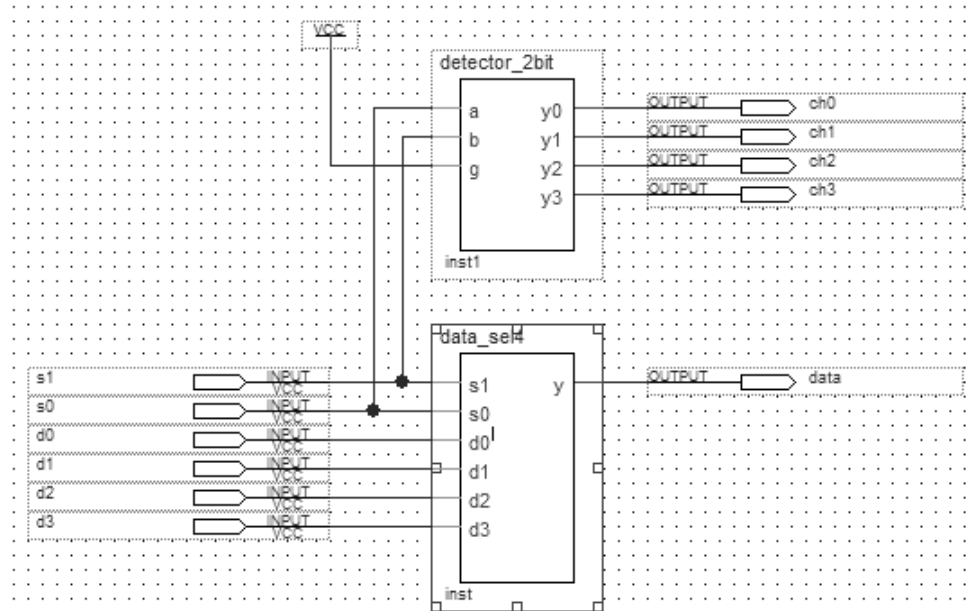


## Unit 5 Creating Hierarchical Logic Circuits

- 5.1 1-out-of-4 data selector (see Lab Manual Example 5-1 & Quartus Tutorial 3 – Hierarchical)
- 5.2 2-channel, 4-bit multiplexer



### 5.3 Multiplexer & decoder



## 5.4 3-bit decoder

