

Digital Design and Computer Architecture

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Final

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This is an open book, open notes take-home exam.

1. [2] What is the **minimum** number of instructions past the current (i.e. the jump) instruction that the jump instruction `j` can jump to? Hint: Think of the extreme case.

2. [2] What is the **maximum** number of instructions past the current (i.e. the jump) instruction that the jump instruction `j` can jump to? Hint: Again, think of the extreme case.

3. [3] You have a pipelined MIPS processor with no bypass hardware. Add the minimal number of nops necessary to the following program to eliminate all hazards.

```
lw $t0, 4($t1)
```

```
add $t2, $t1, $t3
```

```
sub $t0, $t0, $t4
```

```
and $t5, $t2, $t1
```

```
slt $t0, $t6, $t5
```

```
addi $t7, $t5, 42
```

(insert NOPs into code)

4. a) [8] Translate the following procedure into MIPS assembly language. Remember to properly save and restore registers onto the stack, and appropriately decrement and increment the stack pointer. Be sure to comment your code thoroughly.

```
int test(int a) {  
    if (a > 7)  
        return 1;  
    else  
        return (a + test(a+2));  
}
```

b) [3] What is the final returned value from your procedure `test` from part (a) if the argument `a` is -4 when `test` is first called? You may find it useful to draw a picture of the stack during execution.

c) [3] How would your code function if you failed to store `$ra` on the stack? Be specific in your answer.

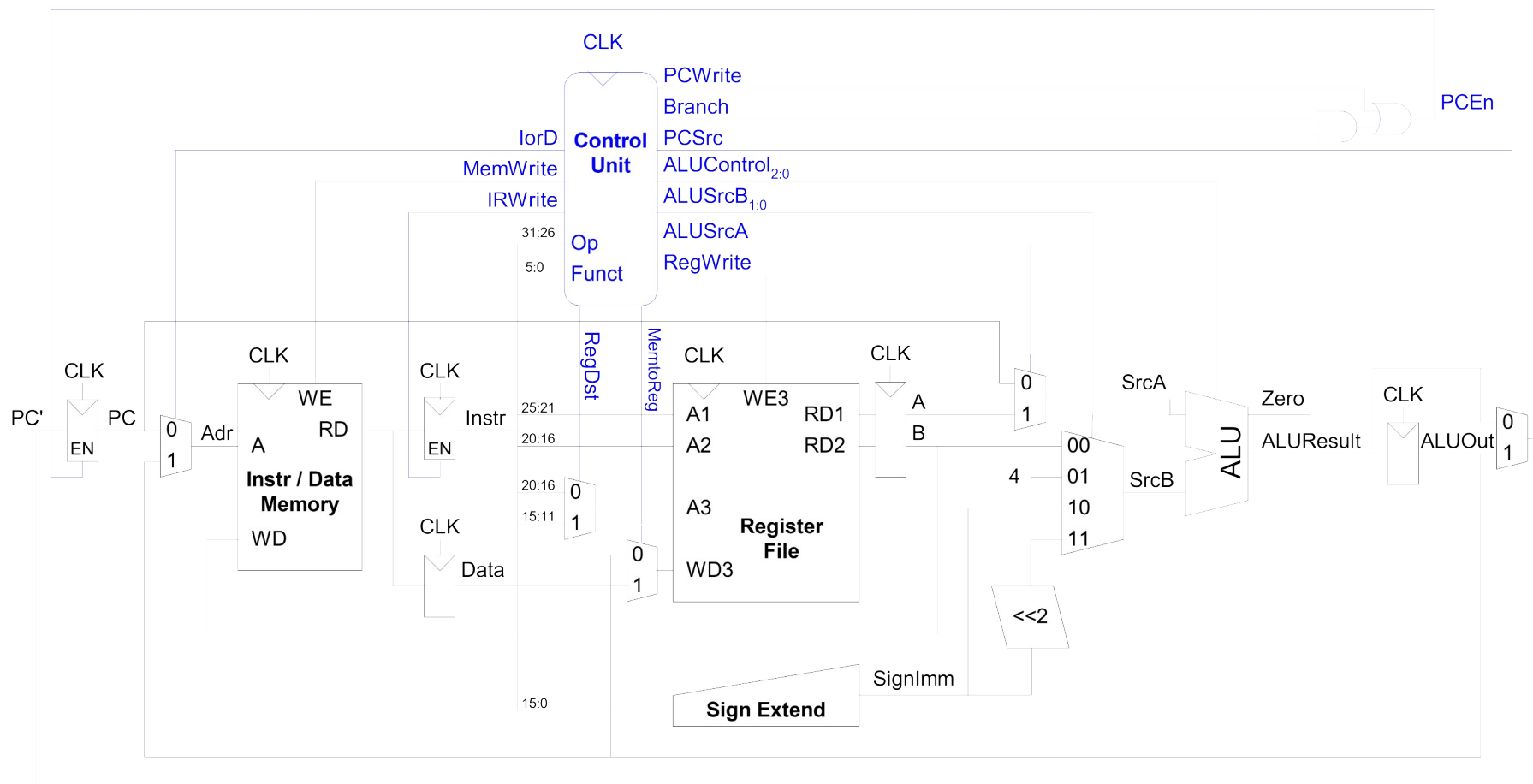
5. You would like to add the `sb` command to your multicycle MIPS processor. Recall that

```
sb $t0, 42($t1)
```

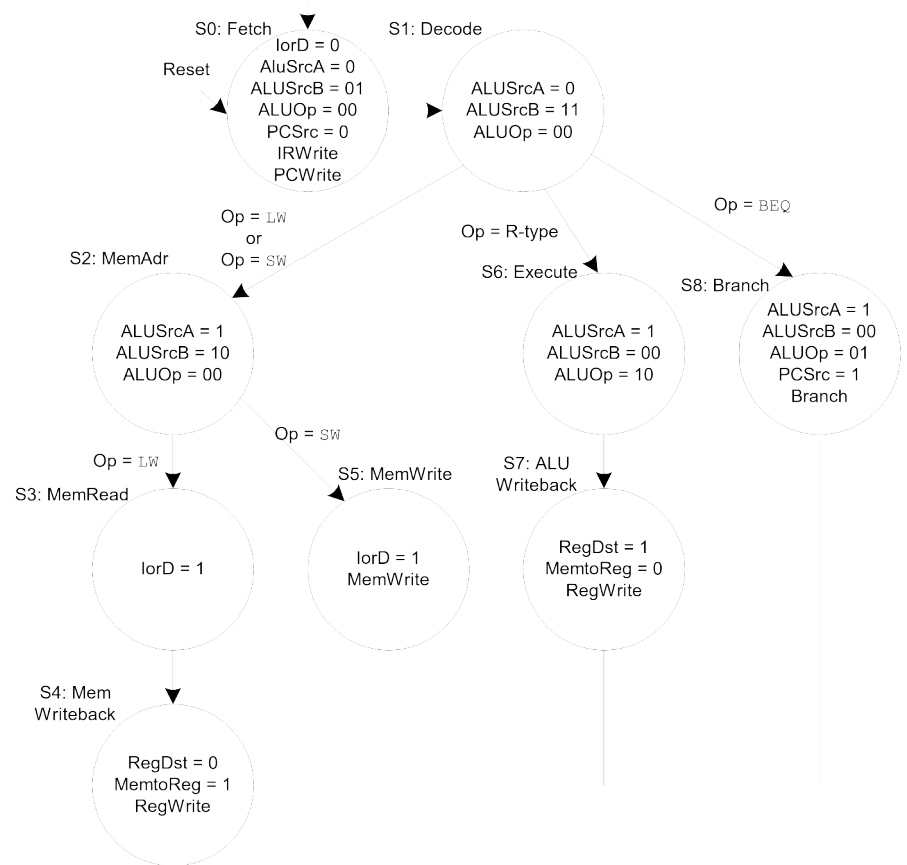
stores the least significant byte of `$t0` into the address 42 bytes beyond the base address in `$t1`.

Suppose you are constrained to use the same memory system that you used in Labs 9 and 10. Recall that this memory system uses a 32-bit wide RAM.

a) [7] Mark up the datapath on the next page with your changes. Do not change the number of bits in existing control signals. Use as few new control signals as possible. Unreadable, incomplete, or messy answers will receive no credit.

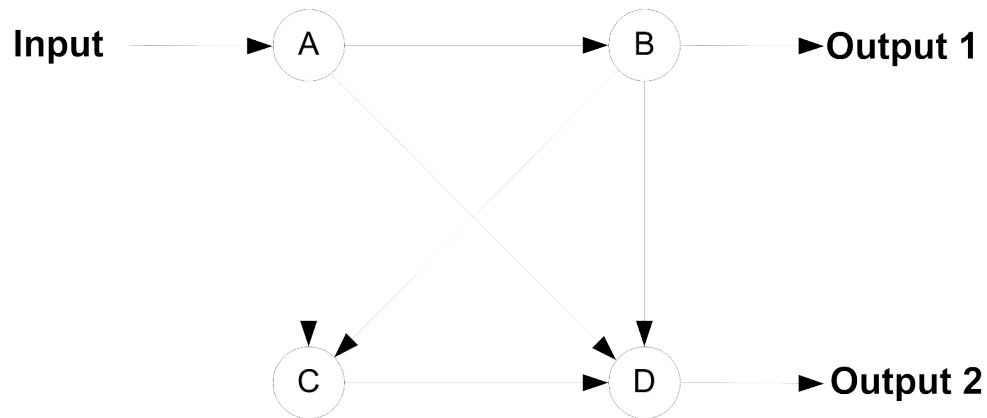


b) [5] Add states to the multicycle FSM shown below to support `sb`. Use as few new states as possible.



(modified state machine)

6. Consider the following combinational circuit. Circles A-D represent combinational circuits, while arrows represent connections between circuits. Each combinational element has a propagation delay of T_{pd} .



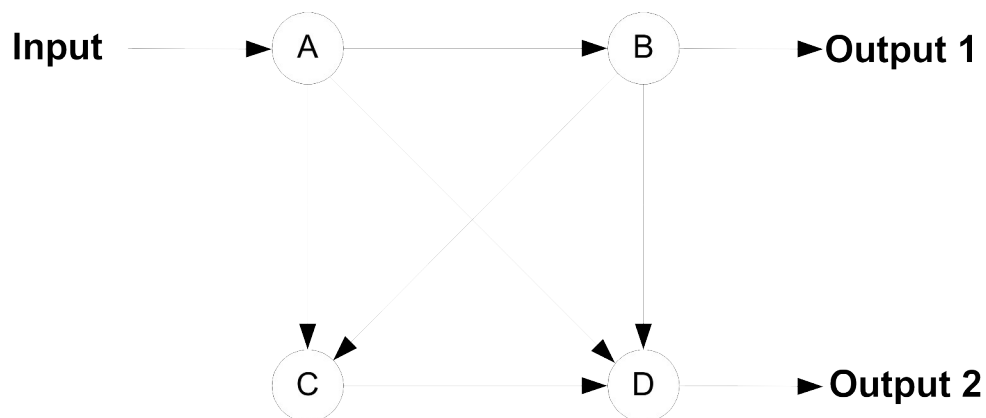
a) [2] Give the latency and throughput of the above circuit.

Latency: _____

Throughput: _____

The following questions deal with pipelined versions of this circuit. Assume that setup, hold, and propagation delays of the registers to be used are all negligible compared to the combinational logic delay.

b) [4] One proposed pipeline structure involves adding registers to the above circuit for a 3-stage pipeline consisting of A in the first stage, B and C in the second stage, and D in the third stage. Mark the locations of registers necessary to implement this plan on the diagram below.



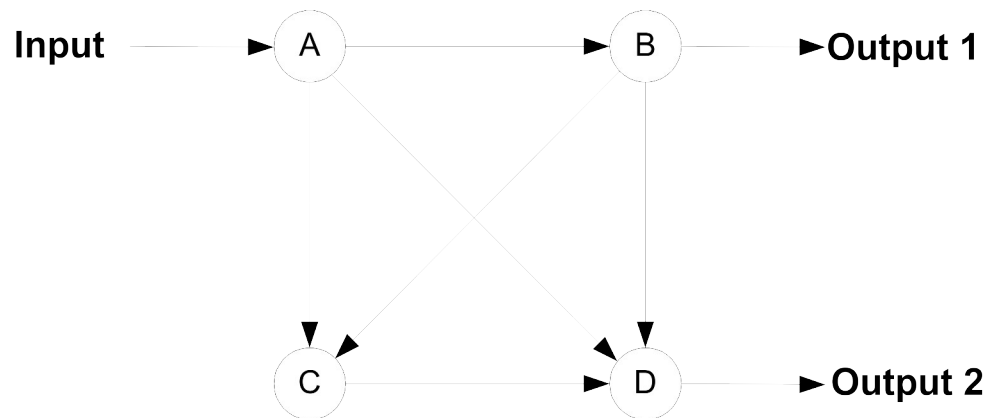
c) [3] Give the minimum clock period for your pipelined version of the circuit in part (b), along with its latency and throughput.

Clock Period: _____

Latency: _____

Throughput: _____

d) [4] Mark, on the copy of the diagram below, locations of the minimum number of registers necessary to pipeline the circuit for maximum throughput. Ensure that every output line contains at least one register.



e) [2] Give the minimum clock period for your maximum-throughput version of the circuit, along with its latency and throughput.

Clock Period: _____

Latency: _____

Throughput: _____

While traveling through Wonderland, Alice encountered the Mock Turtle who proceeded to explain the lessons taught at the school in the sea:

“I only took the regular course.”

“What was that?” inquired Alice?

“Reeling and Writing, of course, to begin with,” the Mock Turtle replied; “and then the different branches of Arithmetic – Ambition, Distraction, Uglification, and Derision. ... There was Mystery, ancient, and modern, with Seaography: then Drawling – the Drawling-master was an old congereel, that used to come once a week: he taught us Drawling, Streching, and Fainting in Coils.”

The poor Mock Turtle was not very good at Arithmetic, so Alice offered to help him with his Floating Point Numbers assignment:

7. [2] Express the following number in IEEE single-precision floating point format (in hexadecimal):

a) -13.5625

Answer _____

8. [3] Add the following IEEE single-precision floating point numbers (shown in binary). You may leave your result in binary form.

1 10000001 10100100000000000001000
+0 10000001 10111000000000000001000

Sum = _____

9. Consider a cache with a line size of L 32-bit words, S number of sets, W ways, and addresses are made up of A bits. Assume that the cache is word addressed, i.e., the low two bits of the address are always 0.

a) [3] Come up with a sequence of addresses for a MIPS processor for which a direct-mapped cache of size 16 words, line size 4 words, outperforms a fully-associative cache with the same line size, using LRU replacement.

b) [2] In terms of the parameters described at the beginning of the problem, what is the cache size in bytes? This number should include just the data portion of the cache.

c) [2] In terms of the parameters above, what is the total number of bytes required to store the tags?

d) [2] What are S and W for a fully-associative cache of size X bytes, with line size L?

e) [2] What is S for a direct-mapped cache of size X bytes, with line size L?

10. You are microarchitecting a MIPS processor and are evaluating the performance of single-cycle, multicycle, and pipelined processors like those described in the text.

Your target application has a mix of 50% R-type instructions, 25% loads, 10% stores, 10% branches, and 5% jumps.

Your circuit designers tell you that the system has the following delays:

- ALU: 900 ps
- Memory: 1000 ps
- Register File read: 400 ps
- Register File write: 400 ps

Other delays such as multiplexers and flip-flops may be neglected in this analysis.

a) [2] What is the cycle time of the single-cycle processor?

T_c single cycle: _____

b) [2] What is the cycle time of the multicycle processor?

T_c multicycle: _____

c) [2] What is the cycle time of the pipelined processor?

T_c pipelined: _____

Suppose the memory system is perfect, i.e., it has a 100% hit rate and there are no data or control hazards. How many millions of instructions per second are executed by:

d) [2] The single-cycle processor?

MIPS: _____

e) [2] The multicycle processor?

MIPS: _____

f) [2] The pipelined processor?

MIPS: _____

Now suppose the data cache is still perfect but the instruction cache has a 5% miss rate. On a cache miss, the processor stalls for 60 ns to access main memory, then resumes normal operation. Taking into account instruction cache misses, how many millions of instructions per second are executed by:

g) [3] The single-cycle processor?

MIPS: _____

h) [3] The multi-cycle processor?

i) [3] The pipelined processor?

MIPS: _____

MIPS: _____

Short Questions

11. Each of the following statements pertains to the miss rate of caches. Mark each statement as true or false. Briefly explain your reasoning; present a counterexample if the statement is false.

a) [3] A 2-way set associative cache always has a lower miss rate than a direct mapped cache with the same line size and total capacity.

(explanation / counterexample)

TRUE / FALSE

b) [3] A 16KB direct mapped cache always has a lower miss rate than an 8KB direct mapped cache with the same line size.

(explanation / counterexample)

TRUE / FALSE

c) [3] An instruction cache with a 32-byte line size usually has a lower miss rate than an instruction cache with 8-byte line size given the same degree of associativity and total capacity.

(explanation / counterexample)

TRUE / FALSE

12. The MuddRaker pipelined processor is designed to support virtual memory, using a single-level page table built from dedicated hardware (fast static RAM and associated logic). It supports 35-bit virtual addresses, 32-bit physical addresses, and 2^{16} -byte (64 KB) pages. Each page table entry contains a physical page number, a valid bit V and a dirty bit D.

a) [3] What is the total size of the page table, in bits?

size of page table (in bits): _____

b) [3] The MuddRaker operating system team proposes reducing the page size from 64 KB to 16 KB, but the hardware engineers objected on the grounds of added hardware cost. Explain their objection.

(brief explanation)